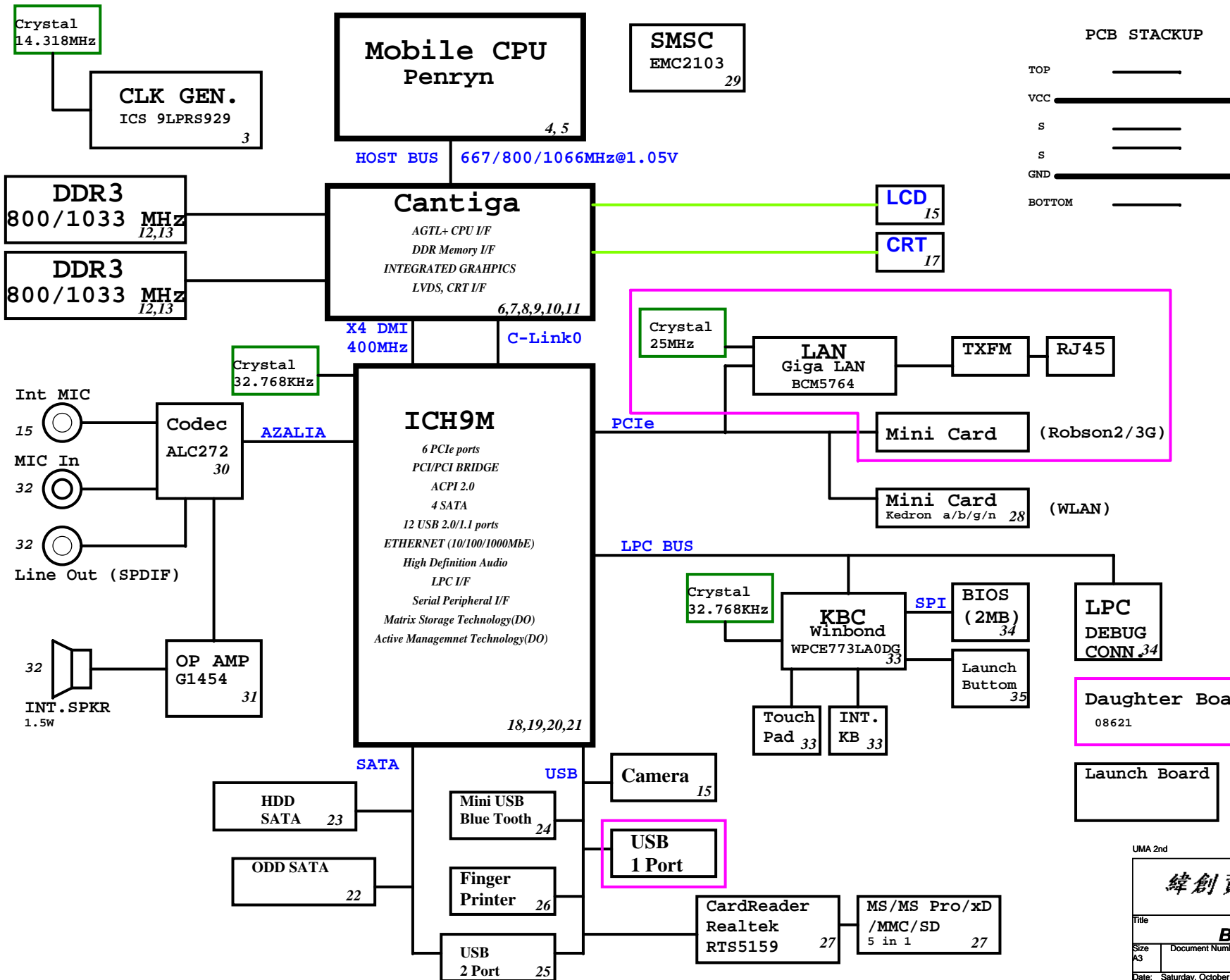


SM30 Block Diagram

Project code: 91.4BT01.001
PCB P/N : 48.4BT01.001
Revision : 08239-SA



SYSTEM DC/DC TPS51125 50	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(7A) 3D3V_S5(7A) 5V_AUX_S5 3D3V_AUX_S5
SYSTEM DC/DC TPS51124 51	
INPUTS	OUTPUTS
DCBATOUT	1D05V_M(16A) 1D5V_S3(12A)
RT9026 52	
1.5V_S3	DDR_VREF_S3 (1.2A)
G9131 52	
3D3V_S0	2D5V_S0 (300mA)
TPS51117 54	
DCBATOUT	1D8V_S0 (9.4A)
CHARGER BQ24750 55	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A
CPU DC/DC ISL6266A 49	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0~1.3V 38A
GFX DC/DC ISL6263 53	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 0~1.3V 6.5A

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage. Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

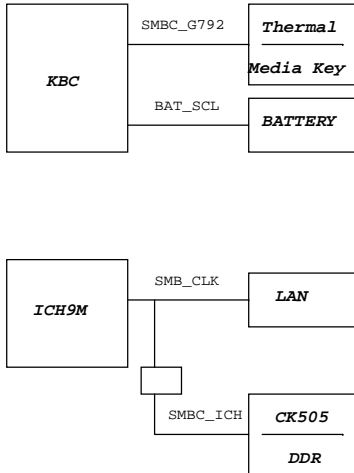
PCIE Routing

LANE1	LAN BCM5764
LANE2	MiniCard WLAN
LANE3	MiniCard(Robson2G/3G)

USB Table

USB	
Pair	Device
0	USB1
1	USB2
2	NC
3	MINIC2(WLAN)
4	CAMERA
5	NC
6	FingerPrint
7	BLUETOOTH
8	NC
9	USB1(IO board)
10	MINIC1(IO BOARD)
11	CARD READER

SMBus



ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

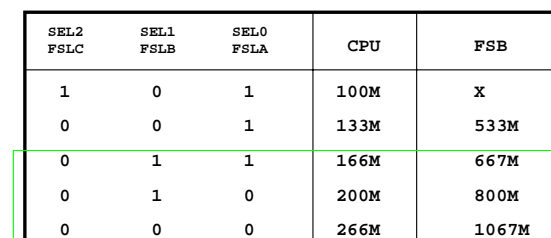
Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disalbed(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCIE are operating simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIE disabled

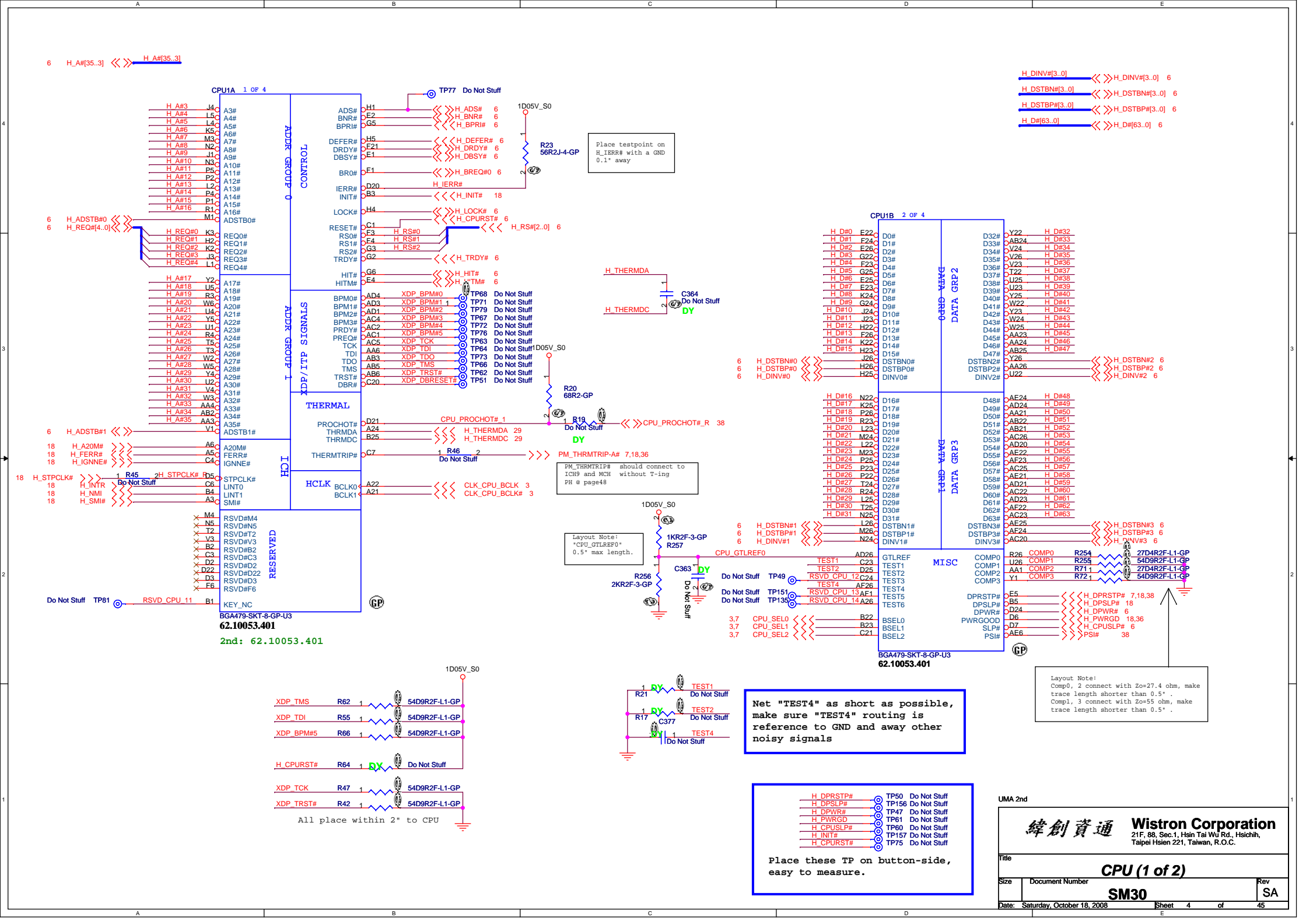
NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

UMA 2nd

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
Reference			
Size A3	Document Number	Rev SA	
SM30			
Date: Saturday, October 18, 2008	Sheet 2 of 45		

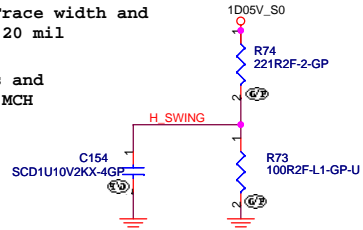


DOC_0	Real Time Frequency
0	Normal
1	Frequency will transition to a preprogrammed value in the I2C
DOC_1	Real Time Frequency
0	Normal
1	Frequency will transition to a preprogrammed value in the I2C

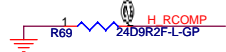


H_SWING routing Trace width and Spacing use 10 / 20 mil

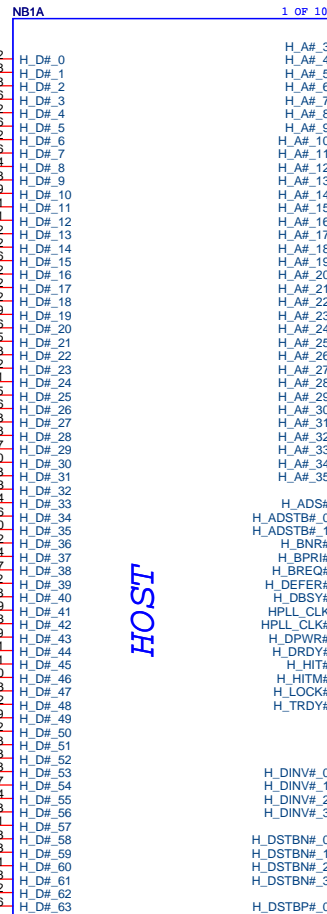
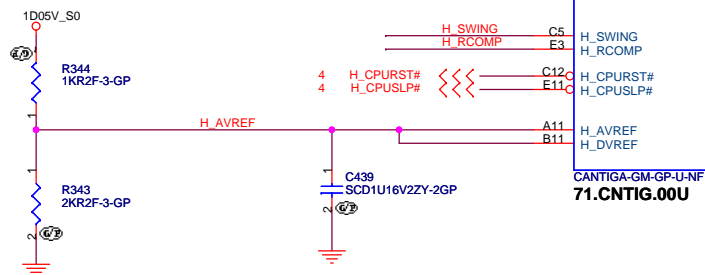
H_SWING Resistors and Capacitors close MCH
500 mil (MAX)



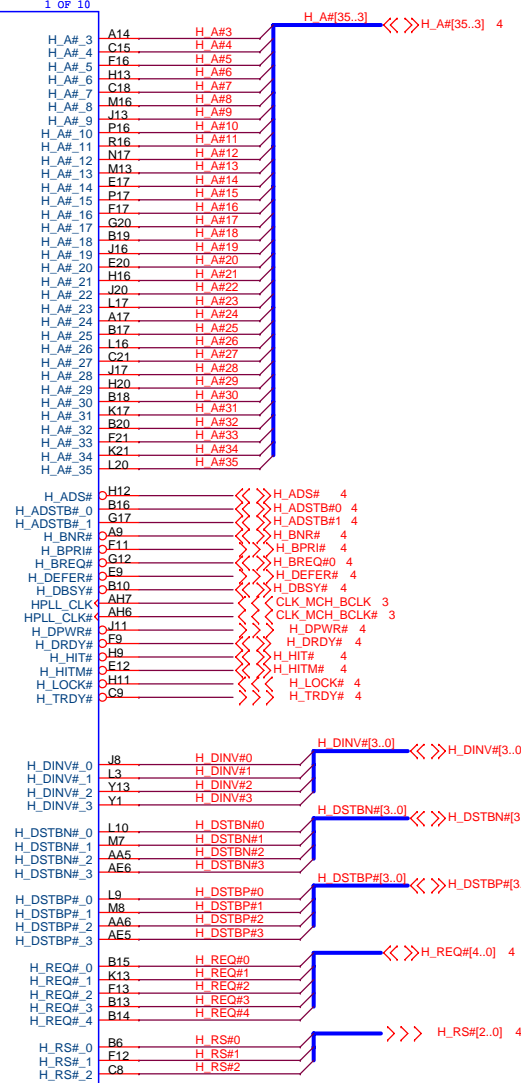
H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



HOST



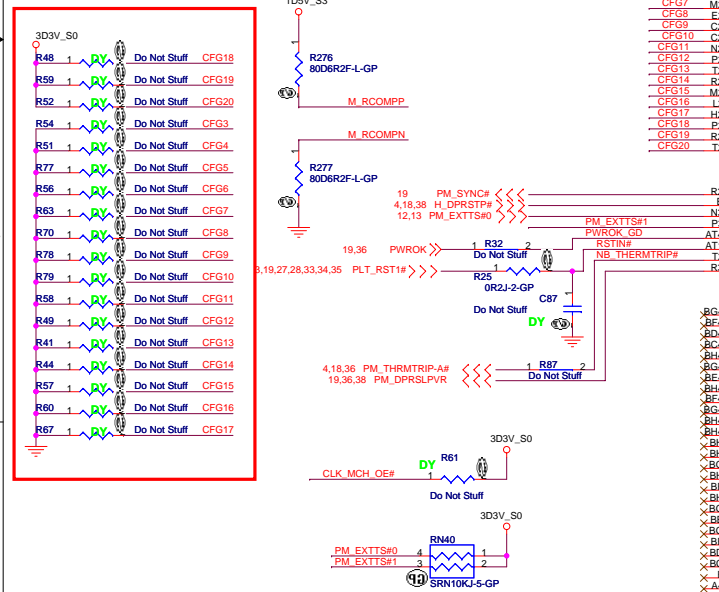
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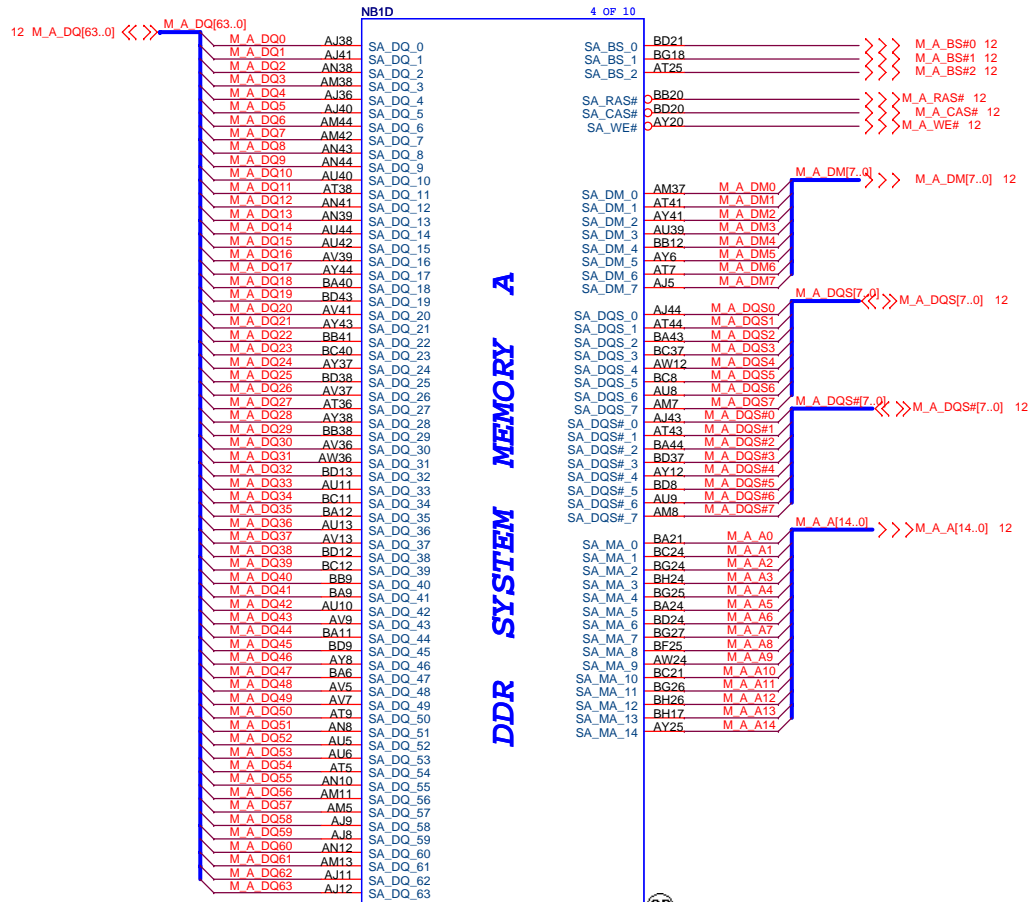
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Title		Cantiga (1 of 6)		Rev
Size	Document Number	SM30		SA
Date:	Saturday, October 18, 2008	Sheet	6	of 45

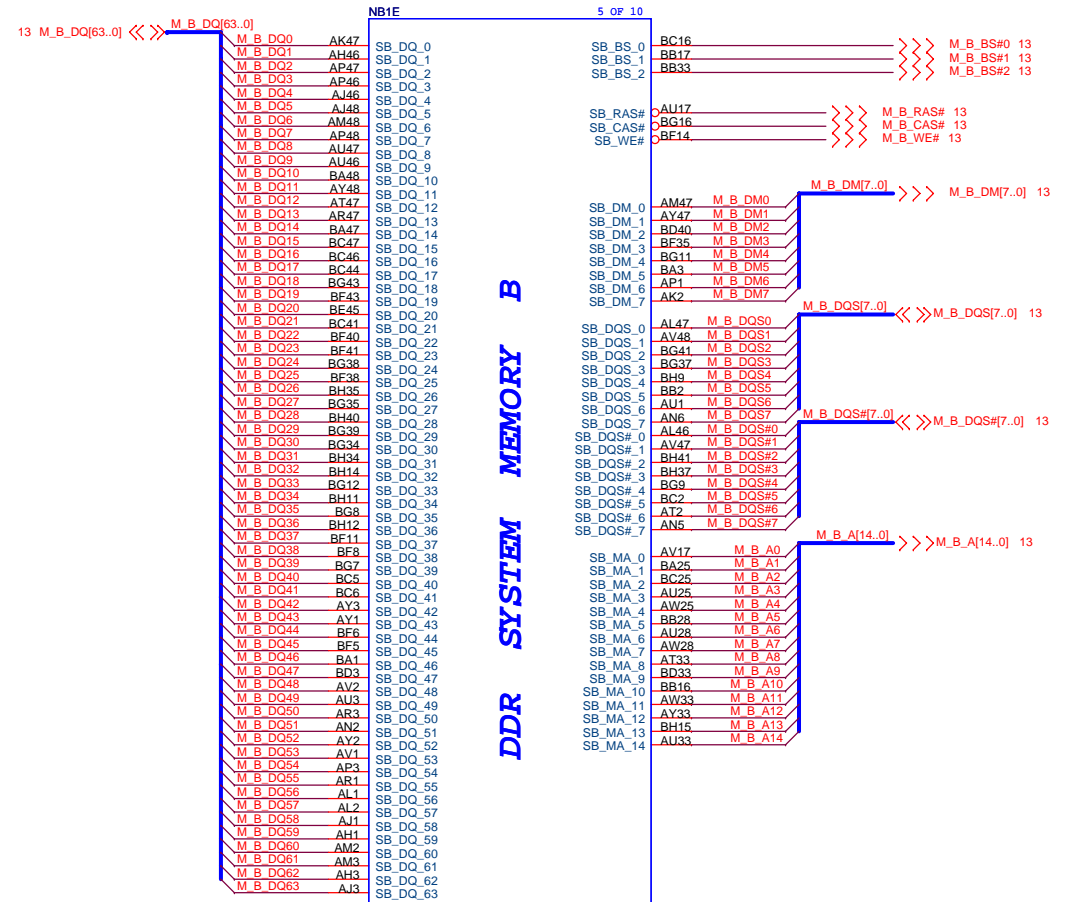
Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1067MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG4:3; 8; 11; 14;15; 17; 18	Reserved
CFG5 (DMI select)	Low = DMI x 2 High = DMI x 4 *
CFG6 (ITPM Host Interface)	High = The ITPM Host Interface is disabled Low = The ITPM Host Interface is enabled *
CFG7 (Intel Management Engine Crypto Strap)	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher site with no confidentiality High = Intel Management Engine Crypto TLS Cipher suite with confidentiality
CFG9 (PCI Express Graphics Lane)	Low = Reverse Lanes, 15->0, 14->1 etc... High = Normal operation:Lane Numbered in Order *
CFG10 (PCI Express Loopback enable)	Low = Enabled High = Disabled *
CFG12 (ALLZ)	Low = ALLZ mode Enabled High = Disabled *
CFG13 (XOR)	Low = XOR mode Enabled High = Disabled *
CFG16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enabled *
CFG19 (DMI Lane Reversal)	Low = Normal operation: Lane Numbered in Order High = Reverse Lanes DMI x 4 mode[MCH->CH]: (0->3, 2->1, 1->2 and 0->3) DMI x 2 mode[MCH->CH]: (3->0, 2->1)
CFG20 (Digital Display Port (SDVO/DP /iHDMI) Concurrent with PCIe)	Low = Only Digital Display Port (SDVO/iHDMI) or PCIe is operational High = Digital Display Port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via the PEG port
SDVO_CTRLDATA (SDVO Present)	Low = No SDVO Card Present High = SDVO Card Present *
L_DDC_DATA (Local Flat Panel (LFP) Present)	Low = LFP Disabled High = LFP Card Present; PCIe disabled
DDPC_CTRLDATA (Digital Display Present)	Low = DisplayPort Disabled High = DisplayPort Device Present

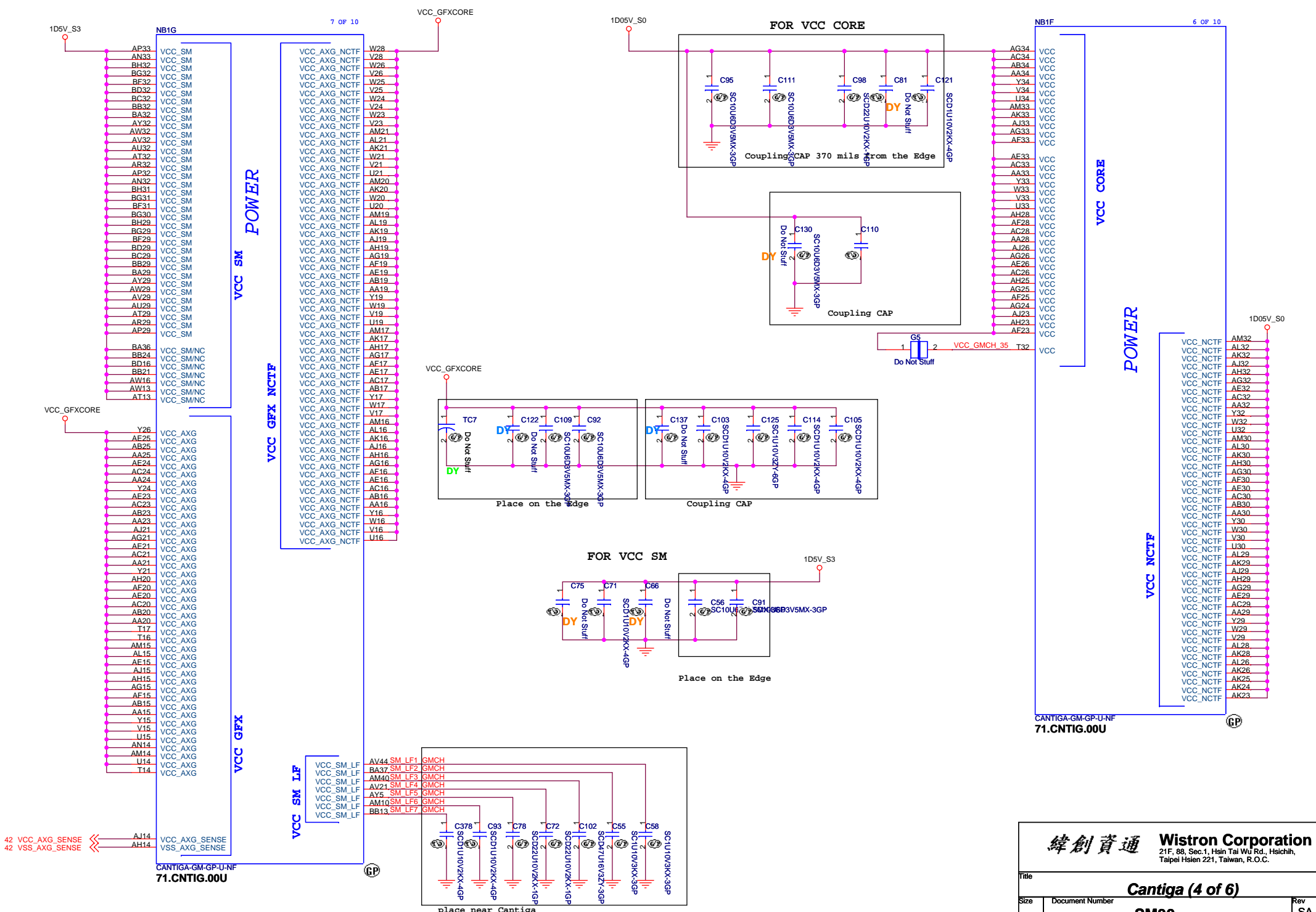


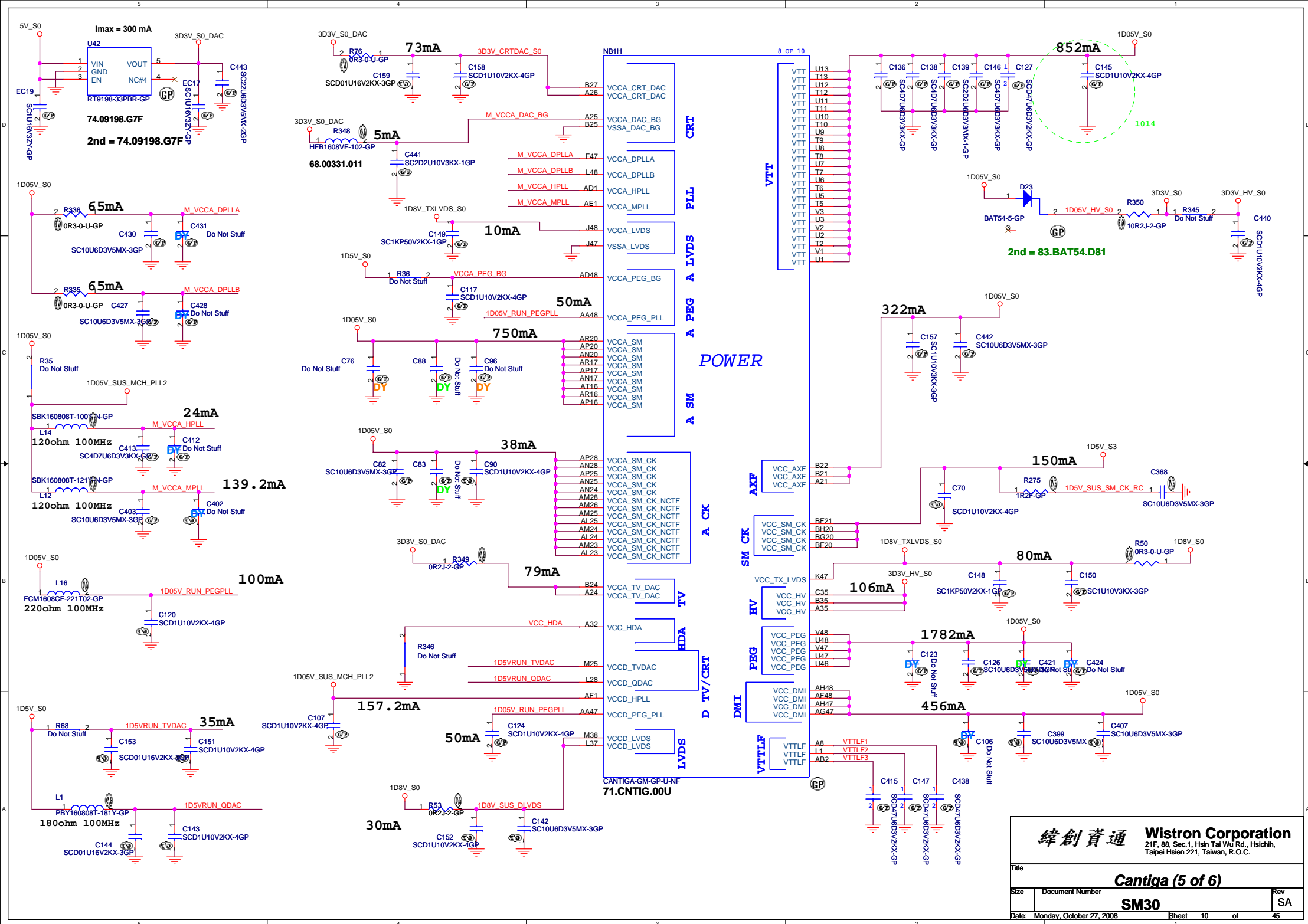


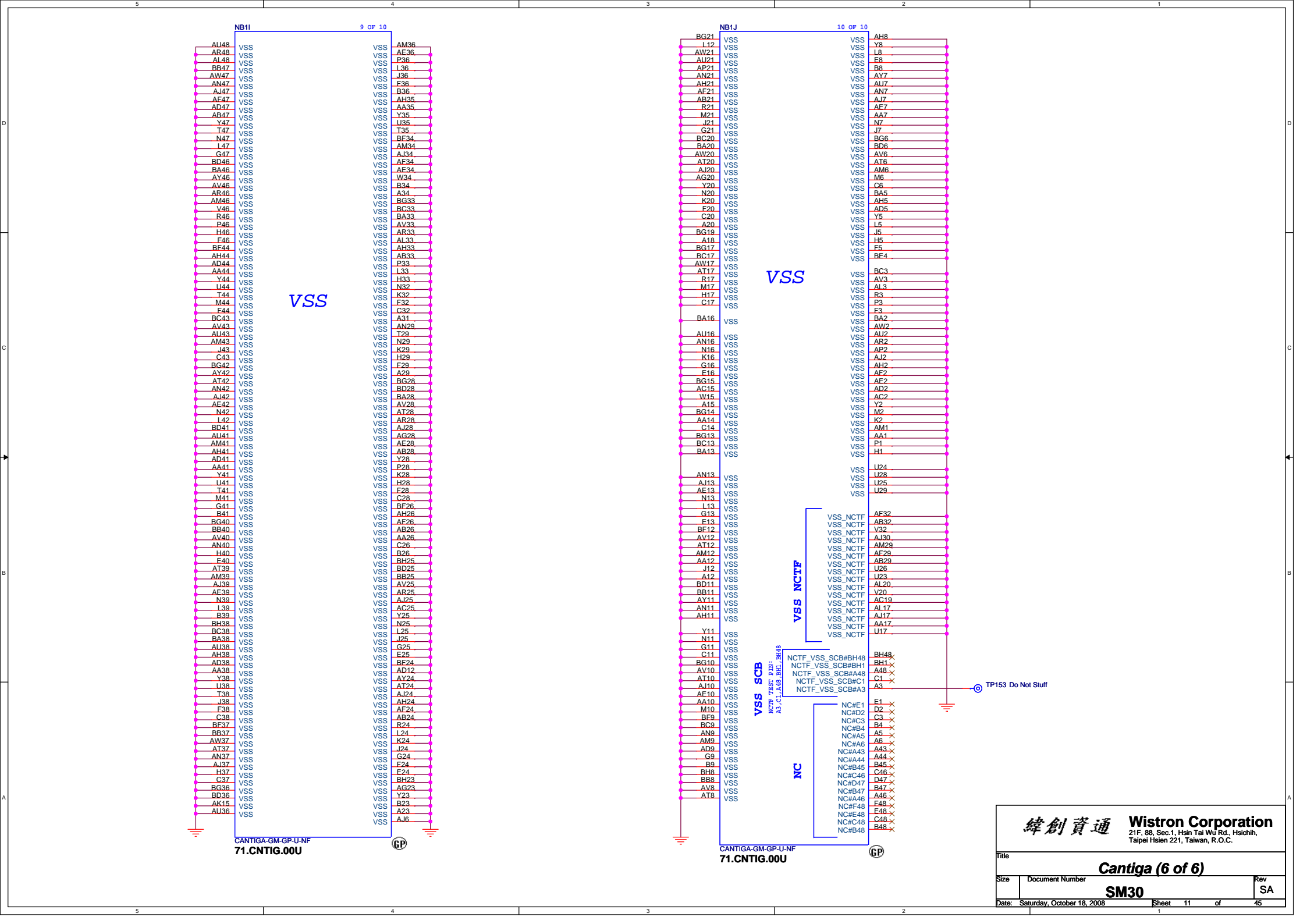
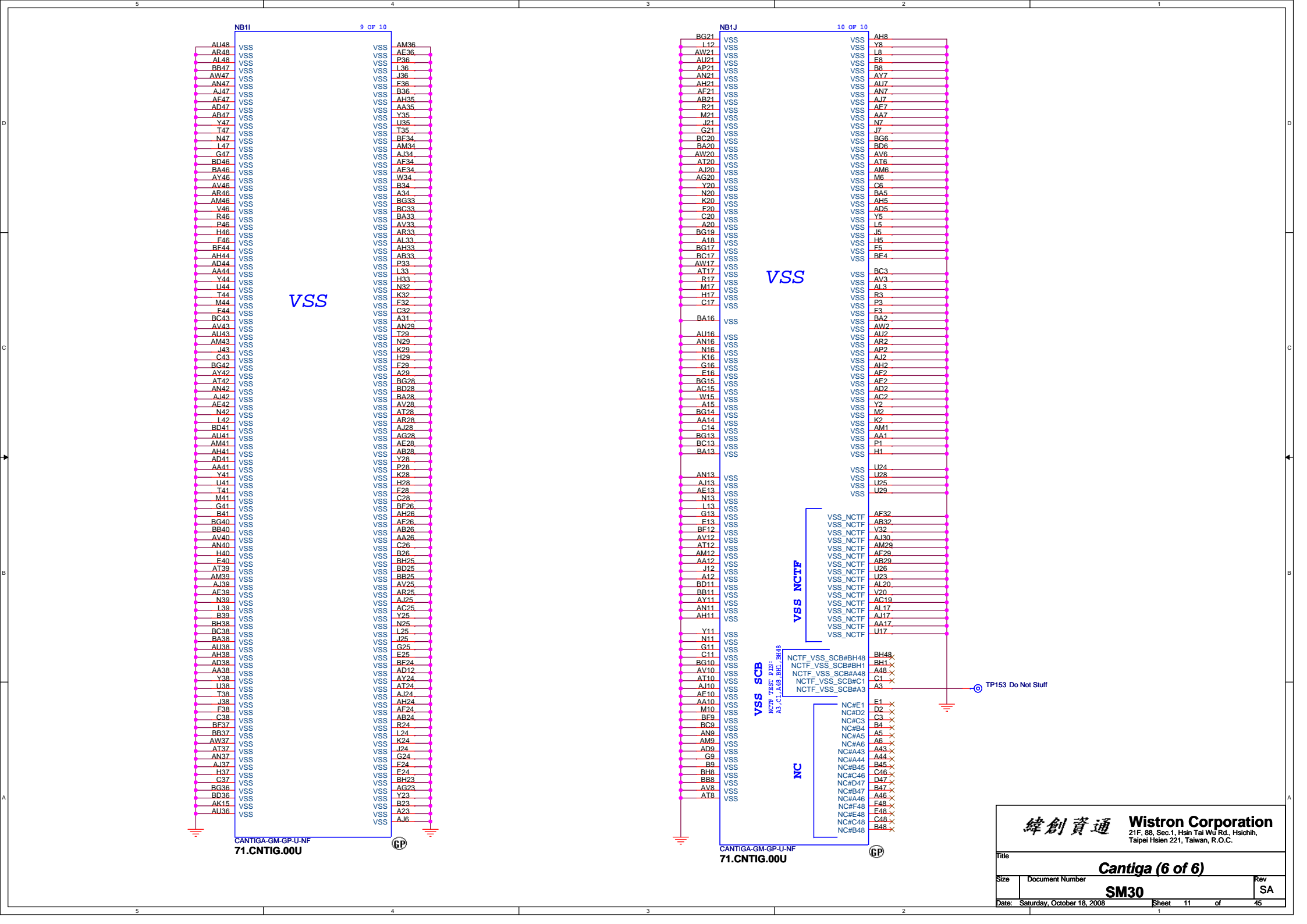
CANTIGA-GM-GP-U-NF
71.CNTIG.00U



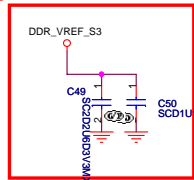
CANTIGA-GM-GP-U-NF
71.CNTIG.00U



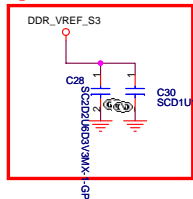
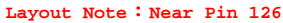




Layout Note : Near Pin 126

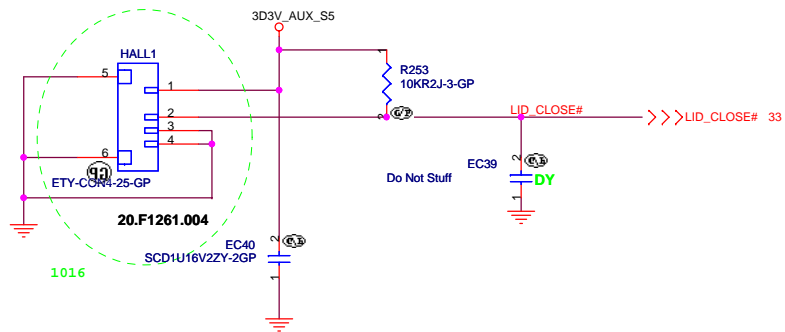


8 M_B_A[14..0] <



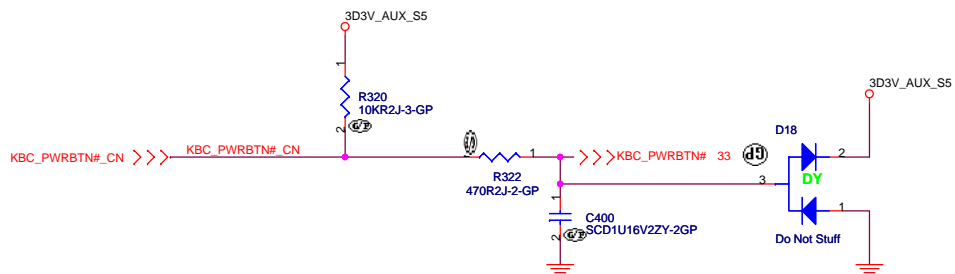
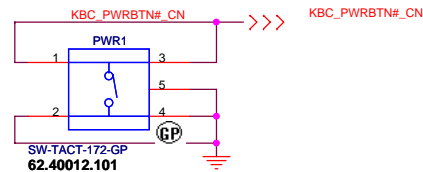
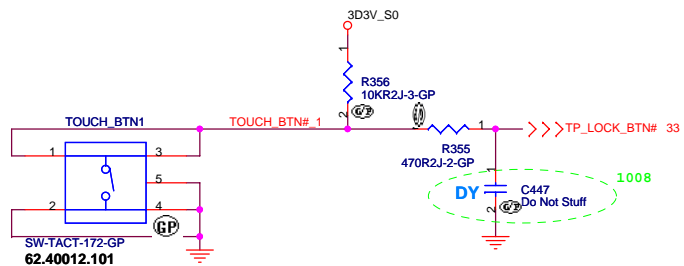
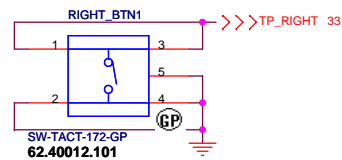
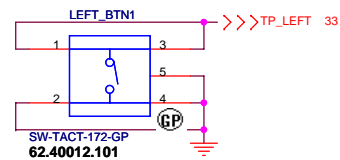
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DDR3 Termination Resistor			
Size	Document Number		Rev
	SM30		SA
Date:	Monday, October 27, 2008	Sheet 13 of	45

Cover Up Switch



74.00268.A7B

74.00268.C7B

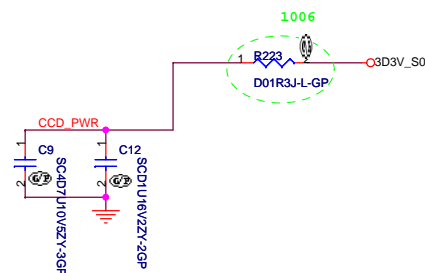
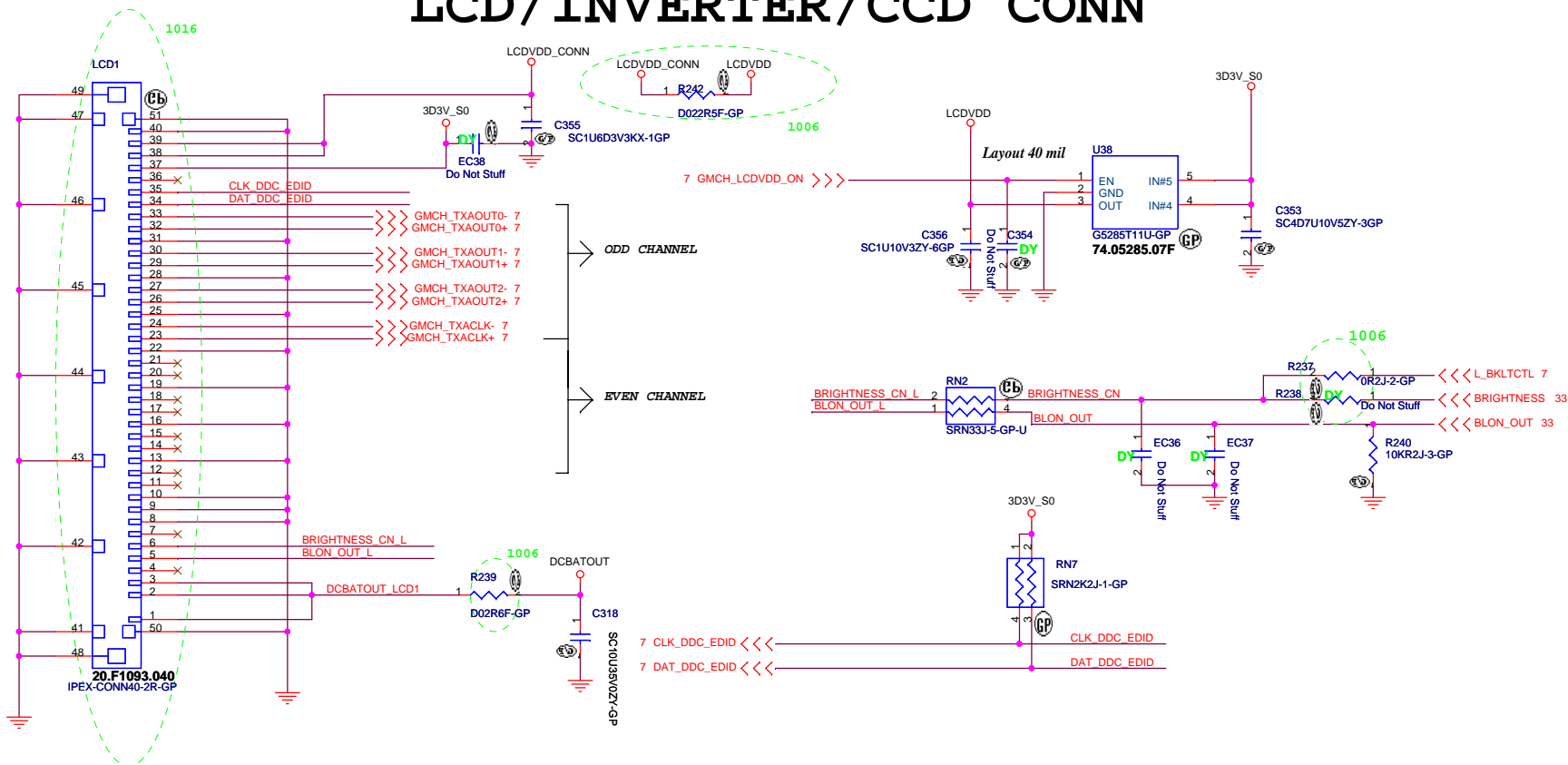


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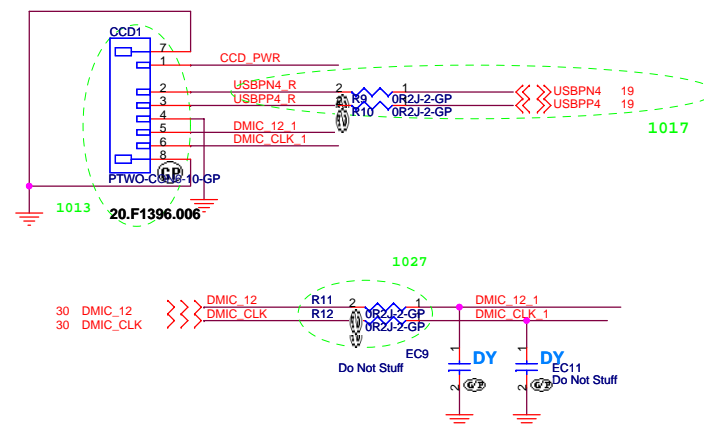
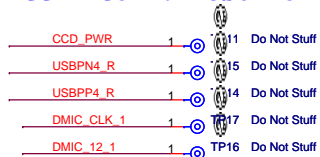
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Title		
SWITCH / Button		
Size	Document Number	Rev
	SM30	SA
Date: Monday, October 27, 2008		
Sheet 14 of 45		

LCD/INVERTER/CCD CONN



CCD1 Conn. Test Point

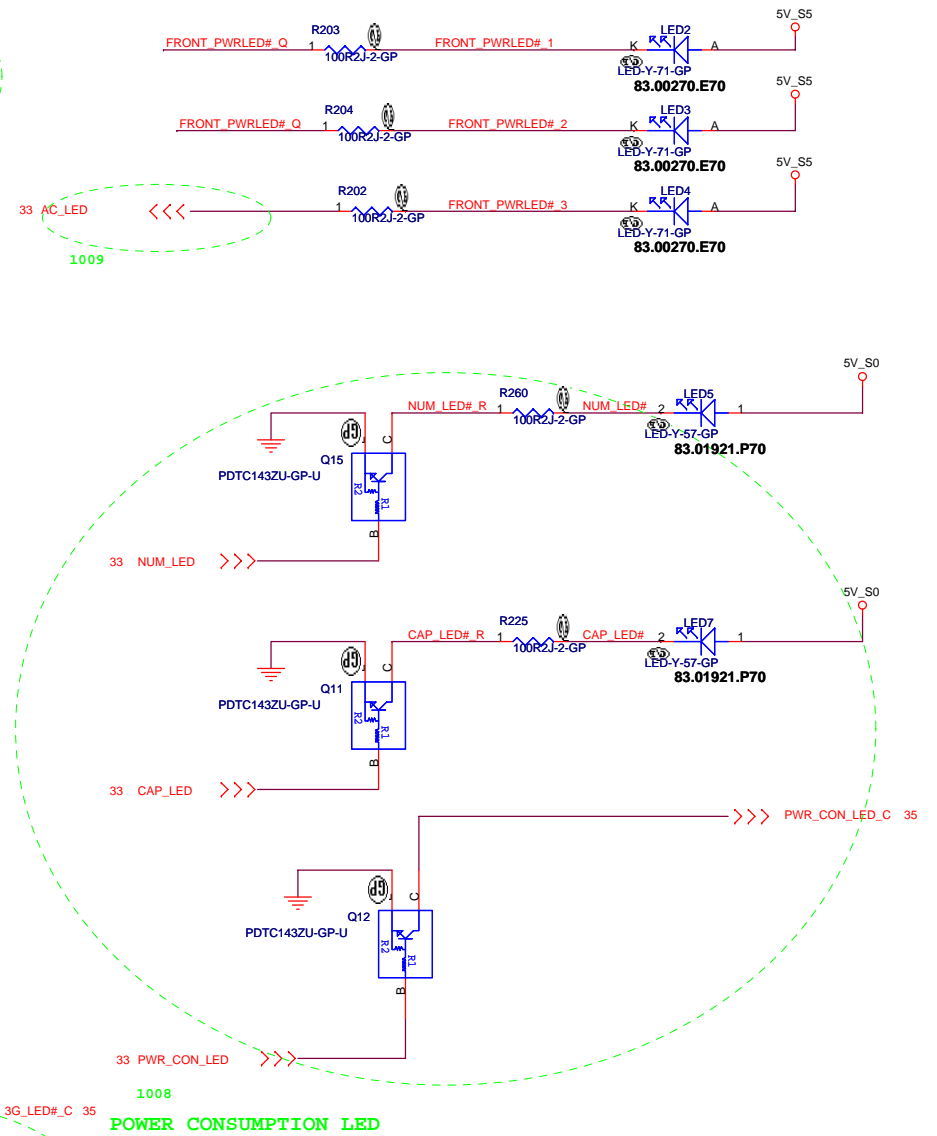
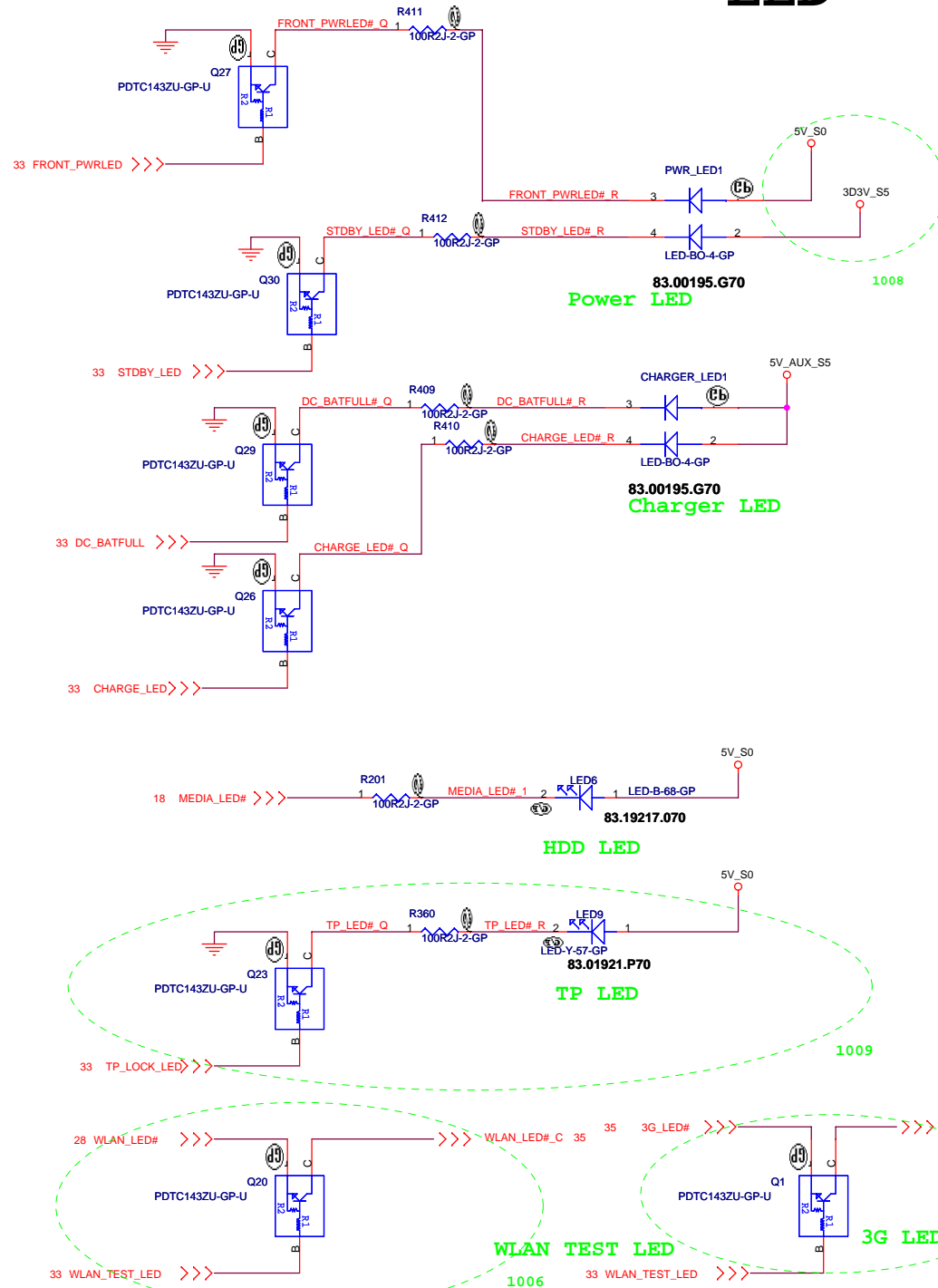


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Title			
LCD CONN			
Size	Document Number		Rev
	SM30		SA
Date:	Monday, October 27, 2008	Sheet 15 of	45

LED



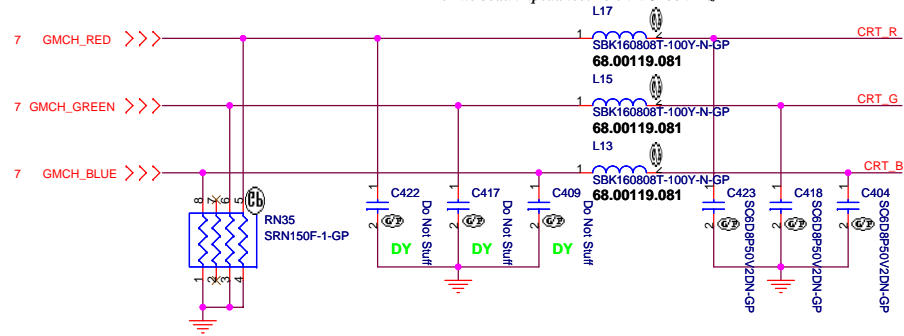
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Title		LED	
Size	Document Number	Rev	SA
Date: Saturday, October 18, 2008		Sheet 16 of 45	

Layout Note:
Place these resistors
close to the CRT-out
connector

Ferrite bead impedance: 10 ohm@100MHz.

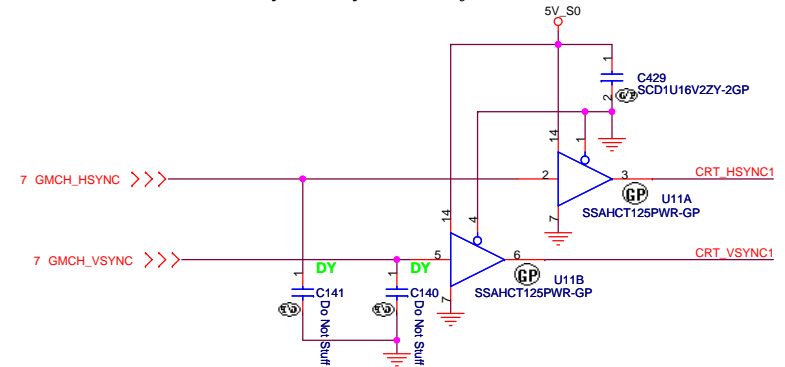


Layout Note:

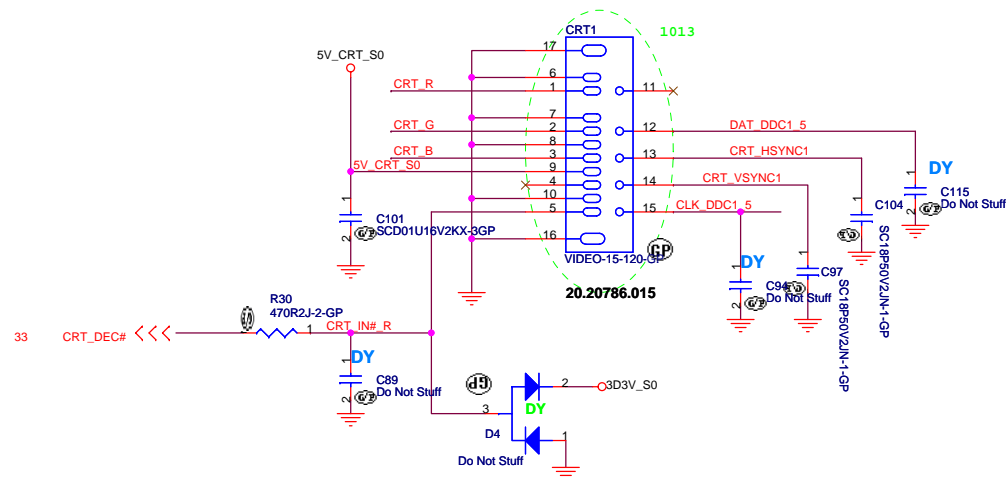
* Must be a ground return path between this ground and the ground on the VGA connector.

Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

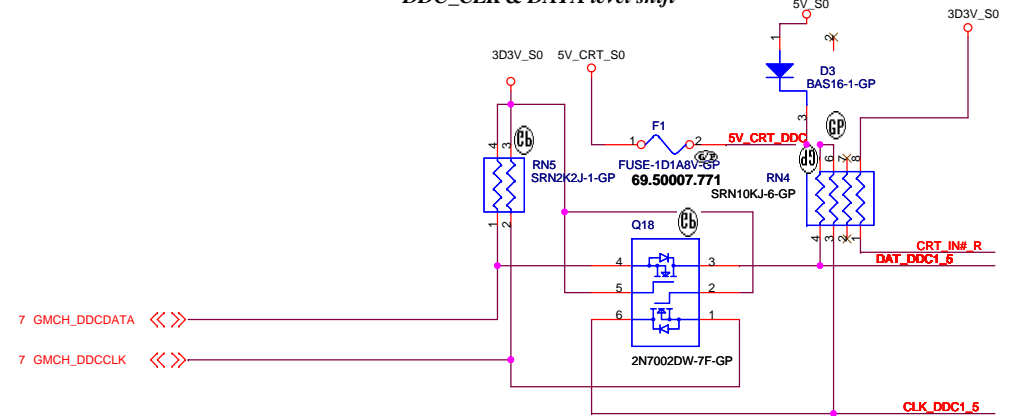
Hsync & Vsync level shift



CRT I/F & CONNECTOR



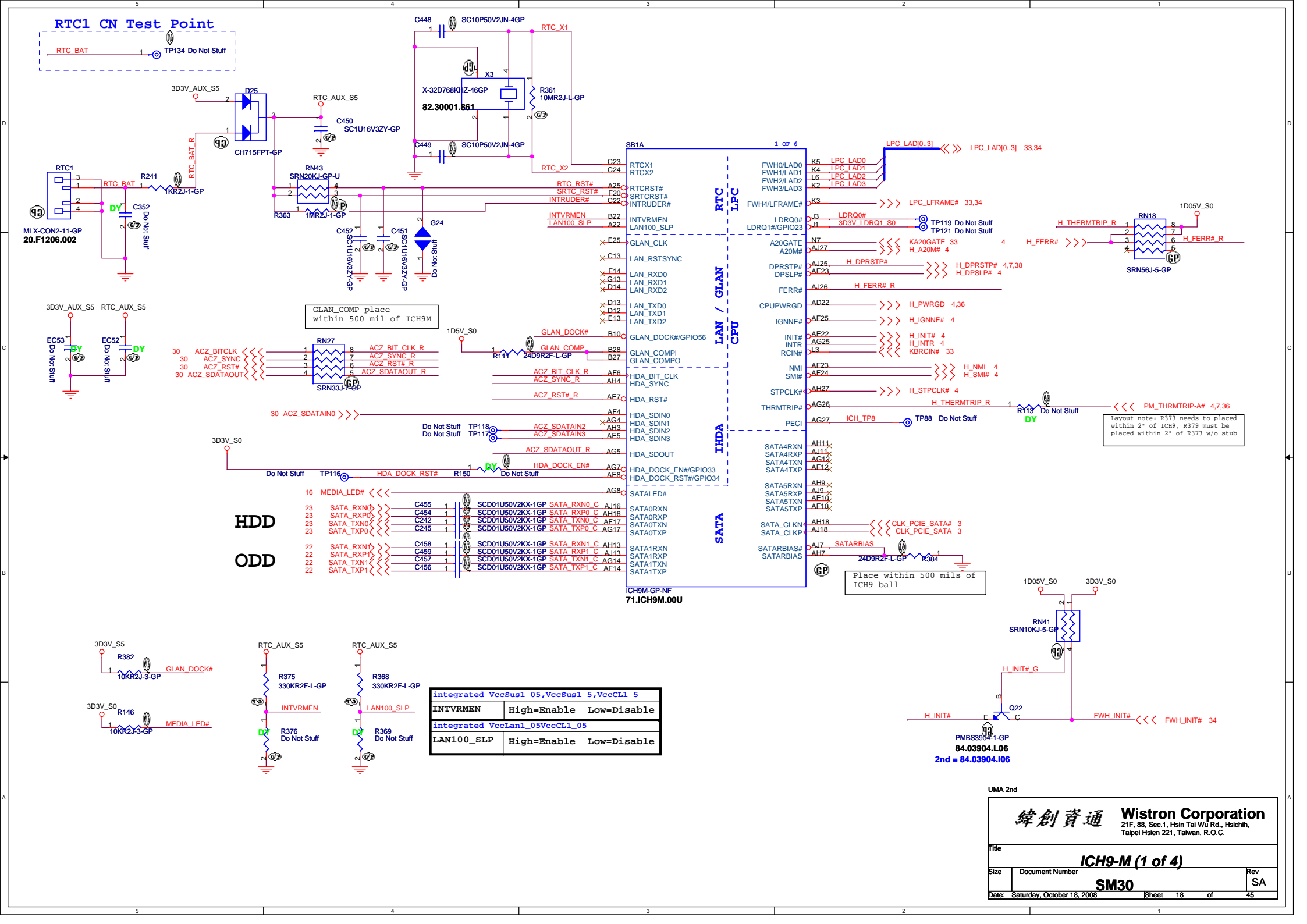
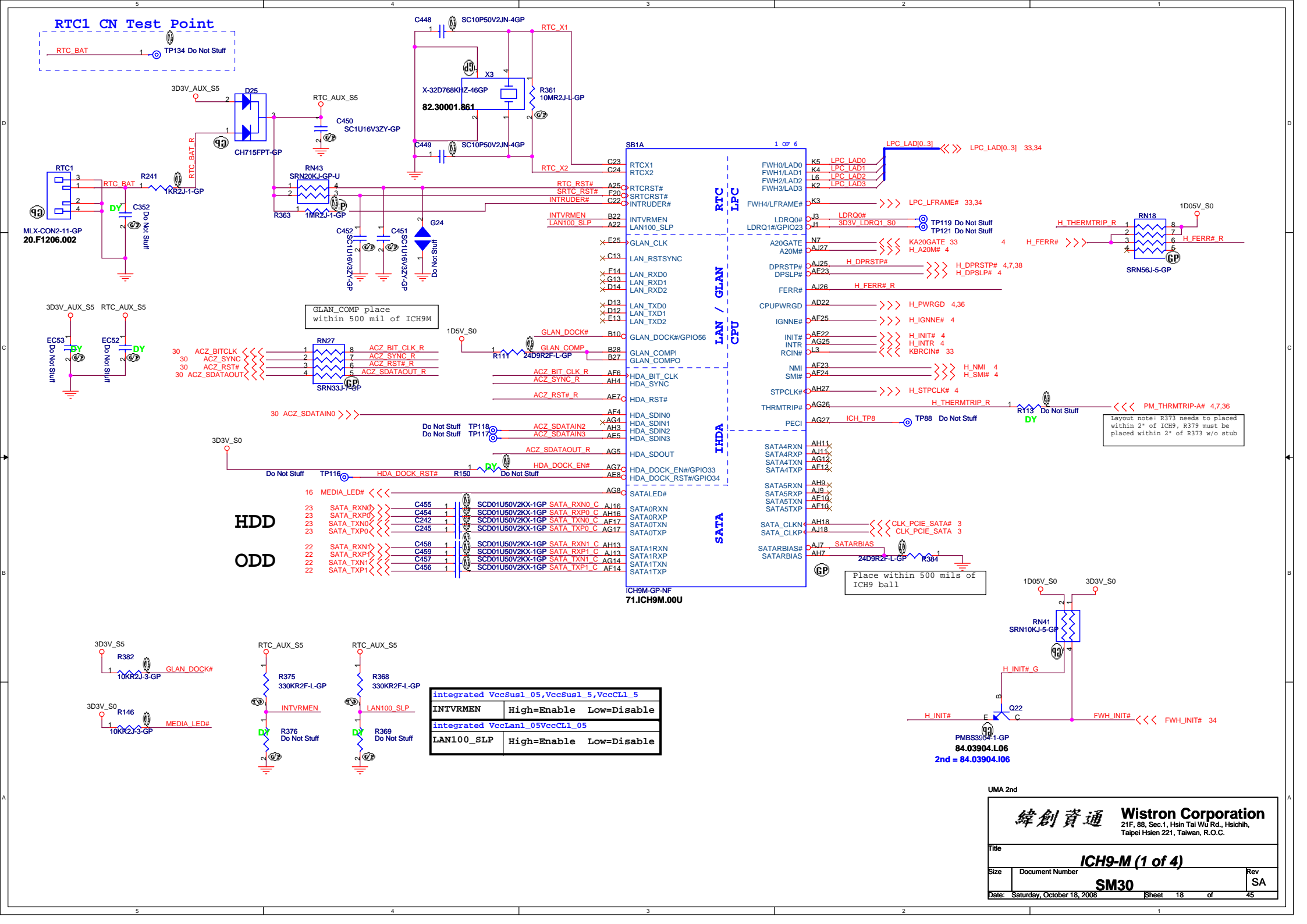
DDC_CLK & DATA level shift

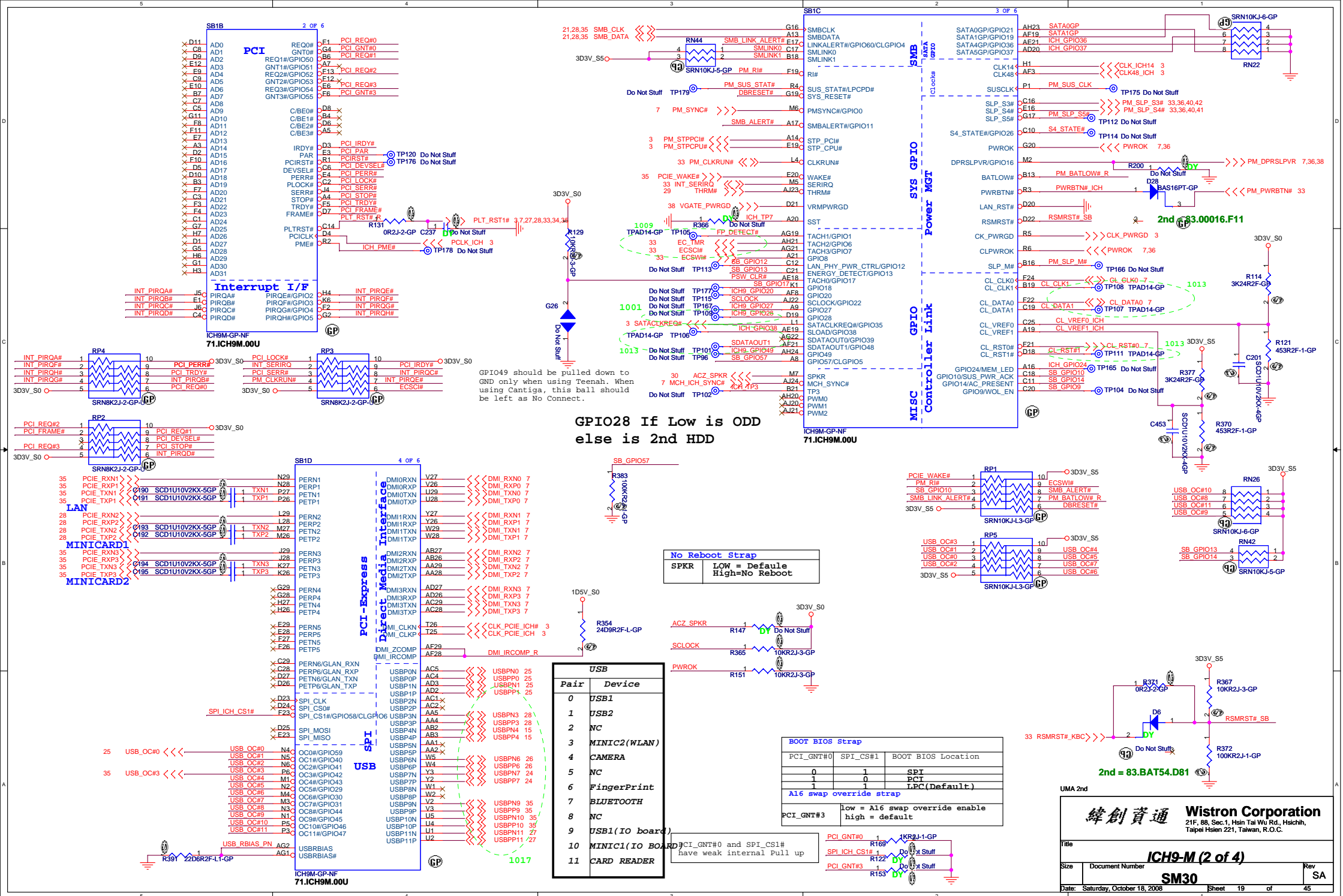


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Taipei Hsien 221, Taiwan, R.O.C.

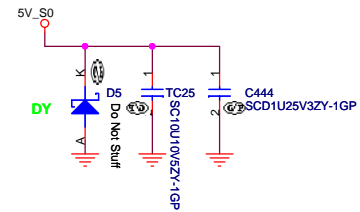
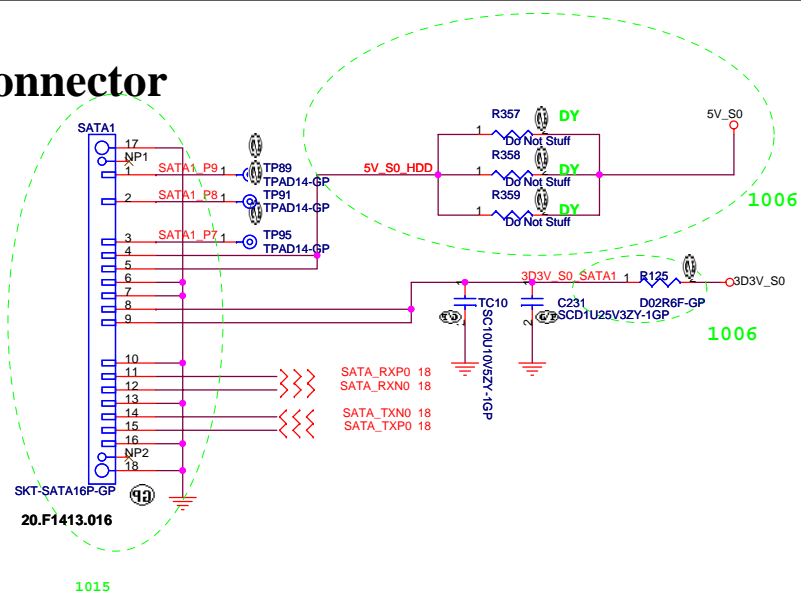
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Size	Document Number	Rev	SA
Date: Monday, October 27, 2008		Sheet 17	of 45



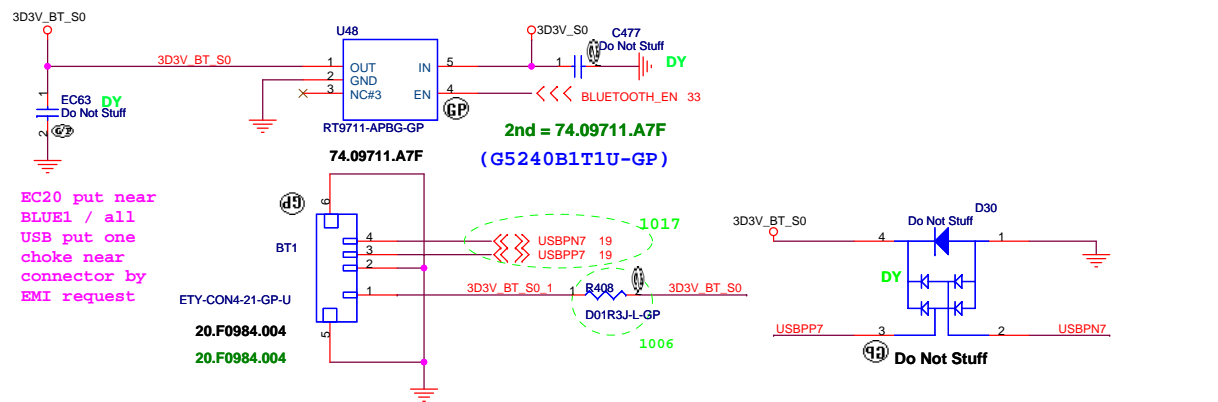




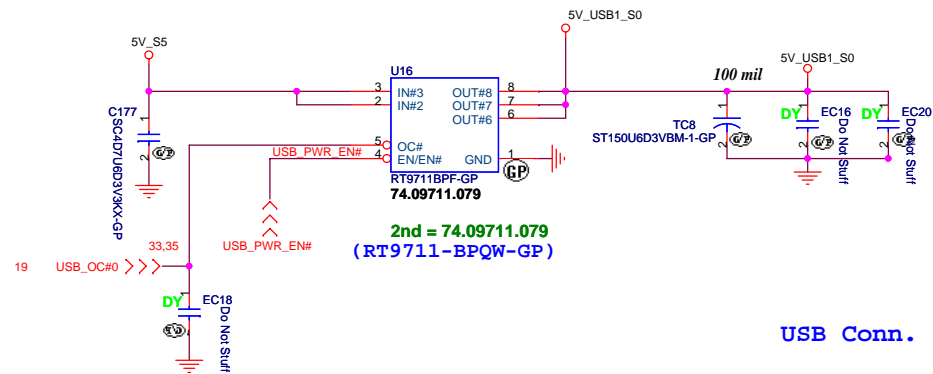
SATA Connector



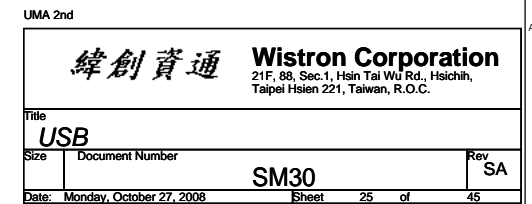
BLUETOOTH MODULE



Need check conn.



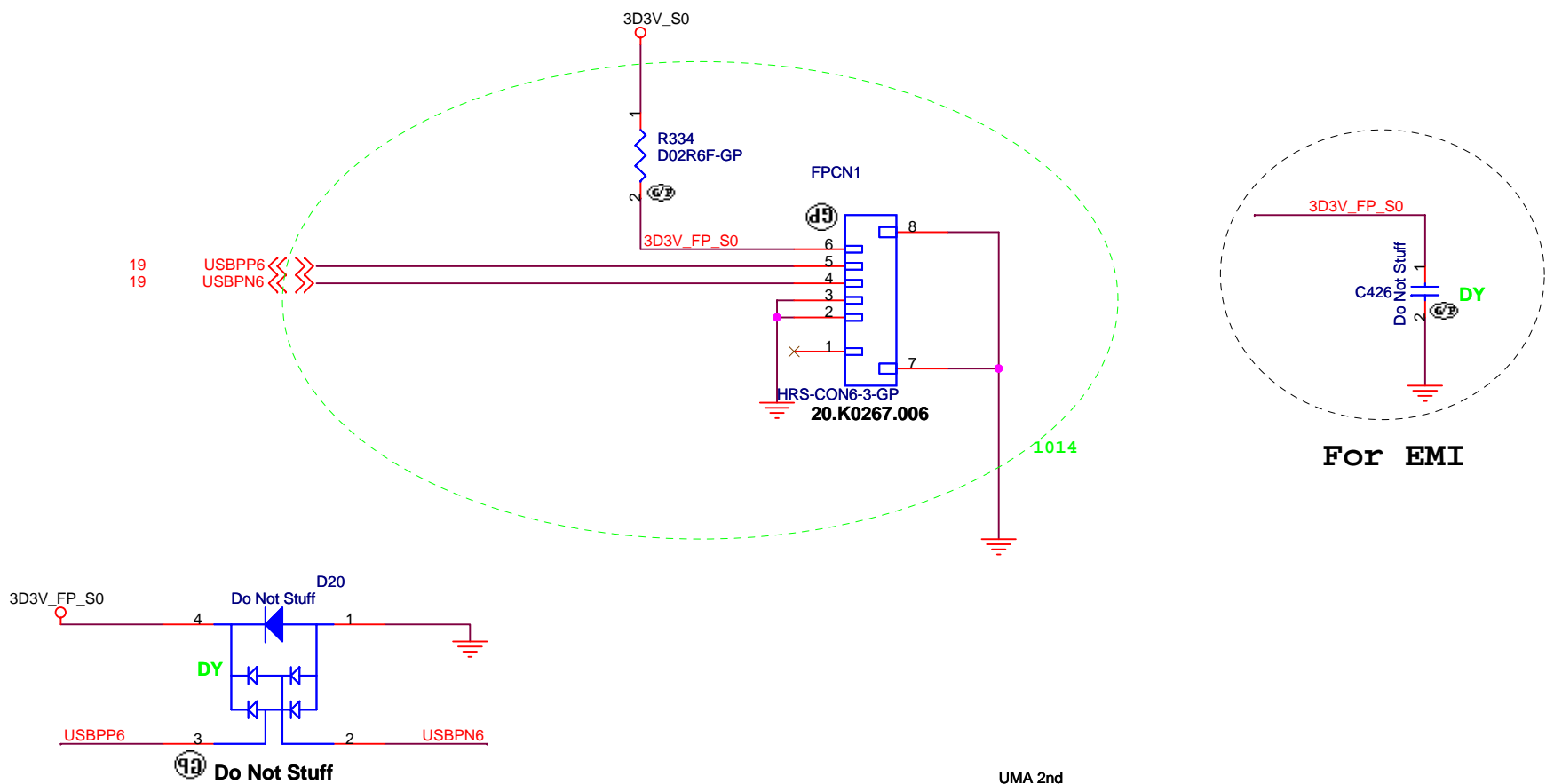
5V_USB1_S0	1	TP37	Do Not Stuff
USBPN0_R	1	TP84	Do Not Stuff
USBPP0_R	1	TP85	Do Not Stuff
USB_1-	1	TP99	Do Not Stuff
USB_1+	1	TP103	Do Not Stuff



Finger printer

FP Conn. Test Point

3D3V_FP_S0 1 TP148 Do Not Stuff
USBPP6 1 TP146 Do Not Stuff
USBP6 1 TP145 Do Not Stuff



UMA 2nd

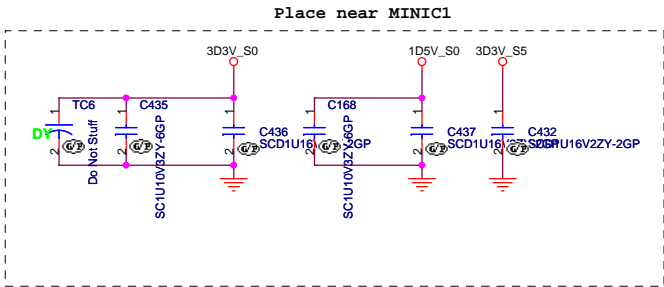
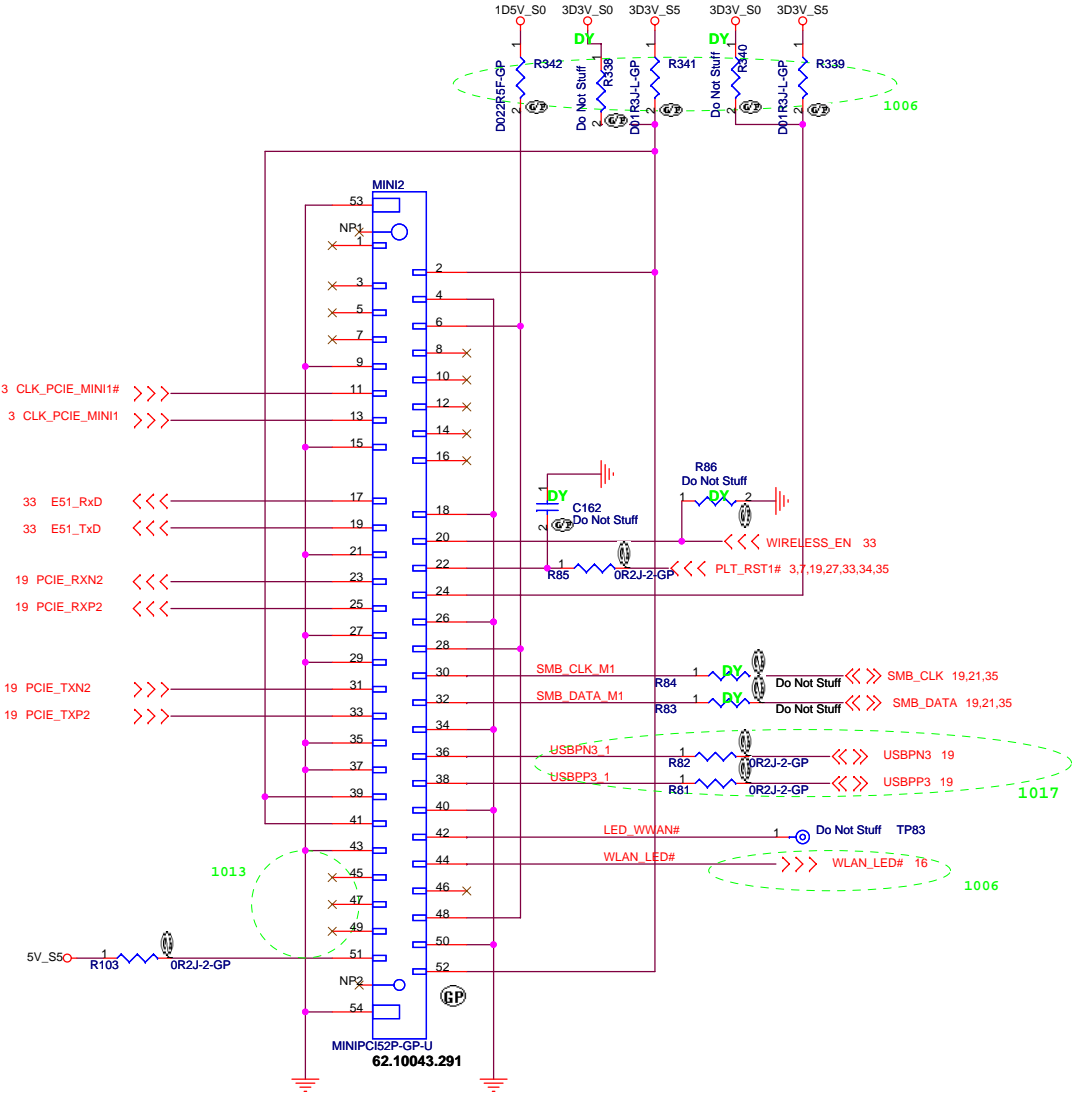
緯創資通

Wistron Corporation

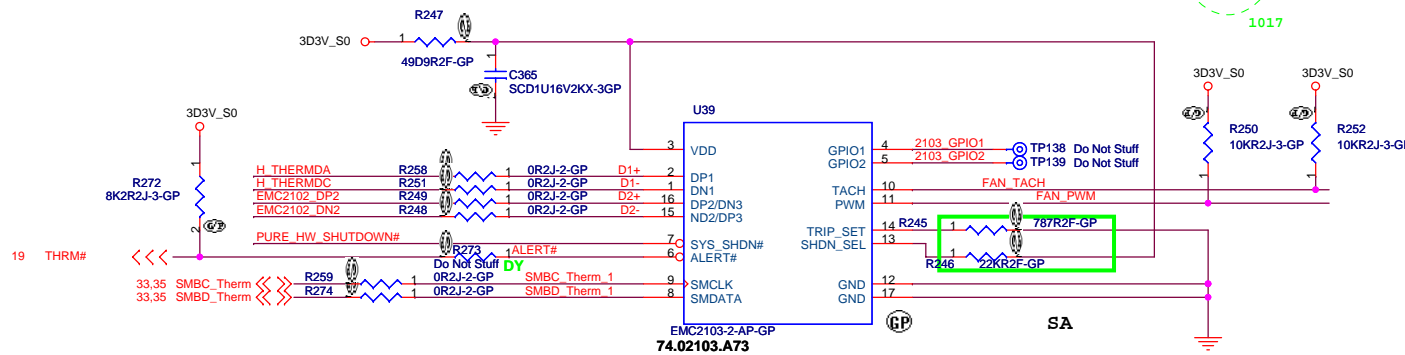
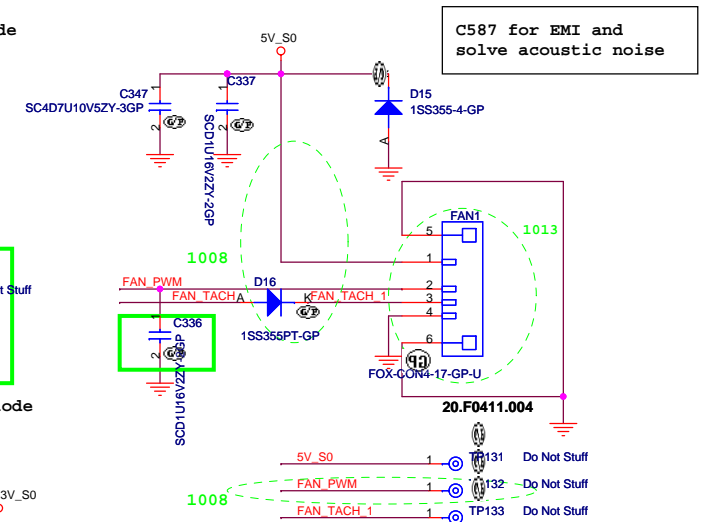
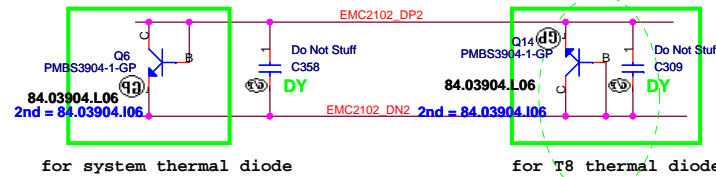
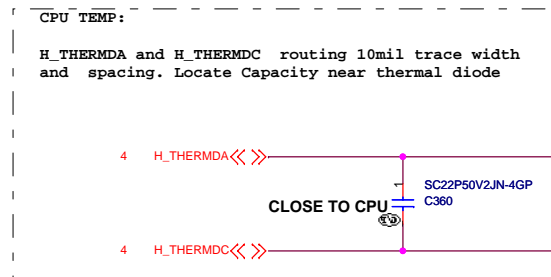
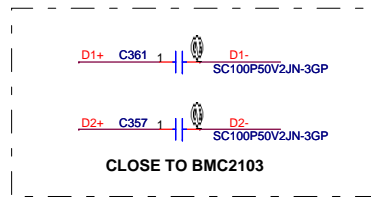
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Finger Printer		
Size	Document Number	Rev
	SM30	SA
Date:	Saturday, October 18, 2008	Sheet 26 of 45

Mini Card Connector(WLAN)



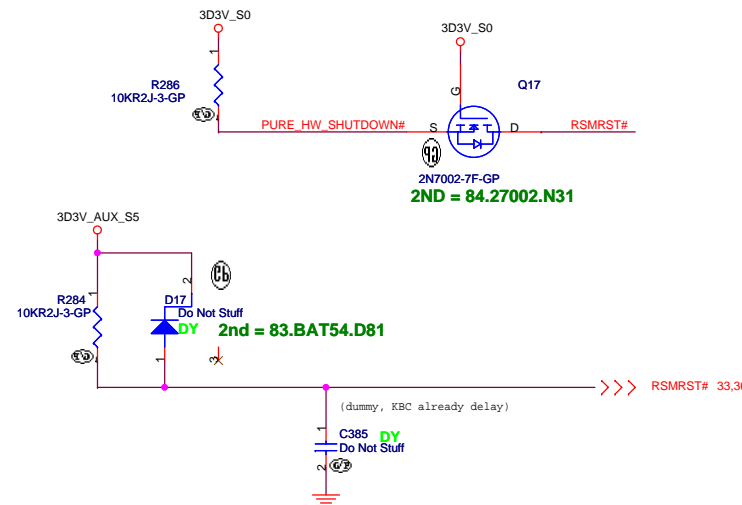
UMA 2nd



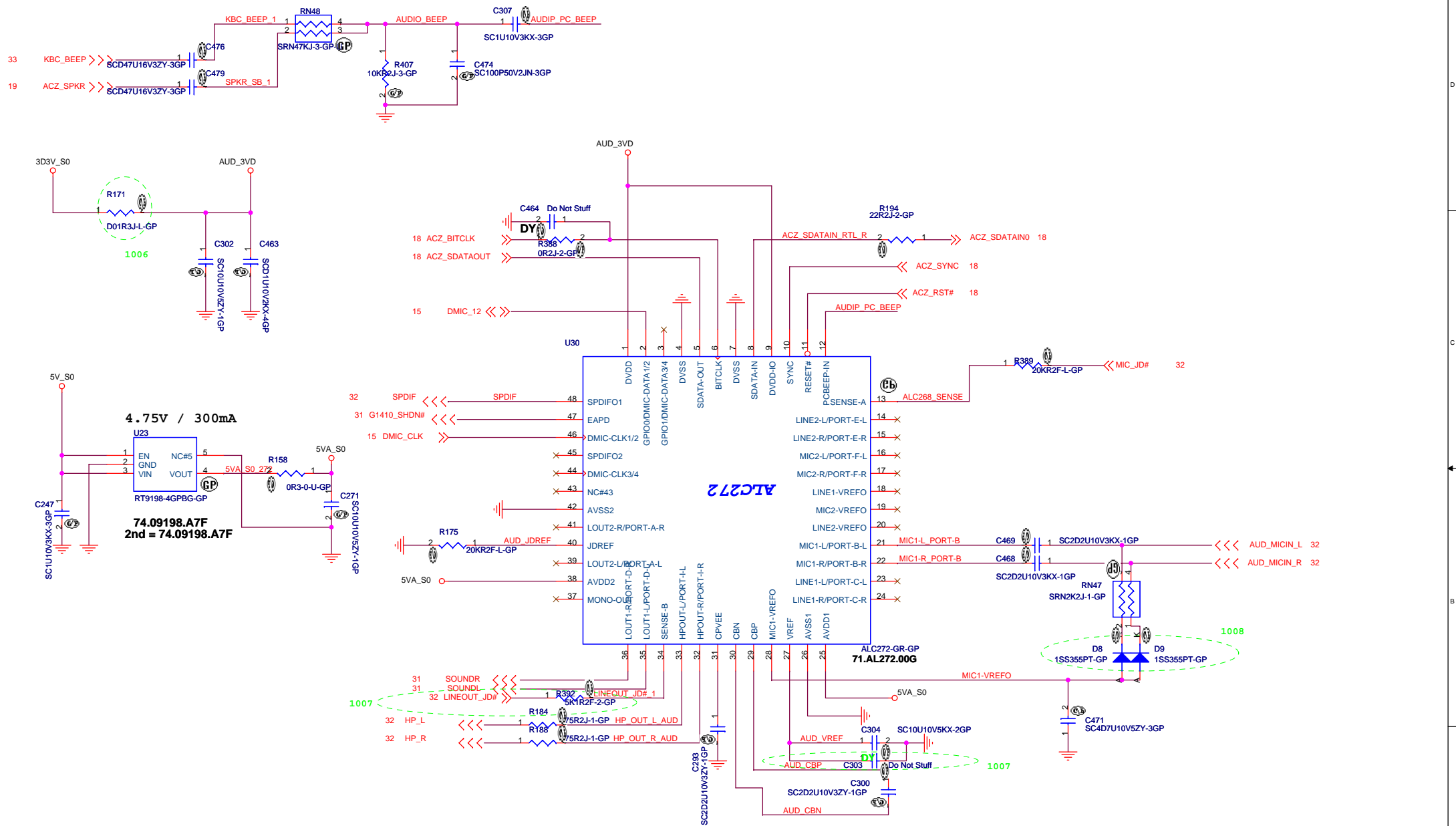
ps. FAN1 POWER TRACE WIDTH MAY BE IN 25 MIL

SHDN SEL	
PULL UP RESISTOR	MODE OF OPERATION
<=4.7K OHM	EXTERNAL DIODE 1 SIMPLE MODE-BETA COMPENSATION DISABLED, REC DISABLED
6.8K OHM	EXTERNAL DIODE 1 DIODE MODE-BETA COMPENSATION DISABLED, REC ENABLED
10K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED, REC ENABLED
15K OHM	INTERNAL DIODE
22K OHM	EXTERNAL DIODE 2 TRANSISTOR MODE-BETA COMPENSATION ENABLED, REC ENABLED
>=33K OHM	EXTERNAL DIODE 1 TRANSISTOR MODE-BETA COMPENSATION ENABLED, REC ENABLED

TRIP SET	
Ttrip(degree)	RSET(1%)
85	562
86	604
87	649
88	698
89	750
90	787
91	845
92	909
93	953
94	1020
95	1100



UMA 2nd



UMA 2nd

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.

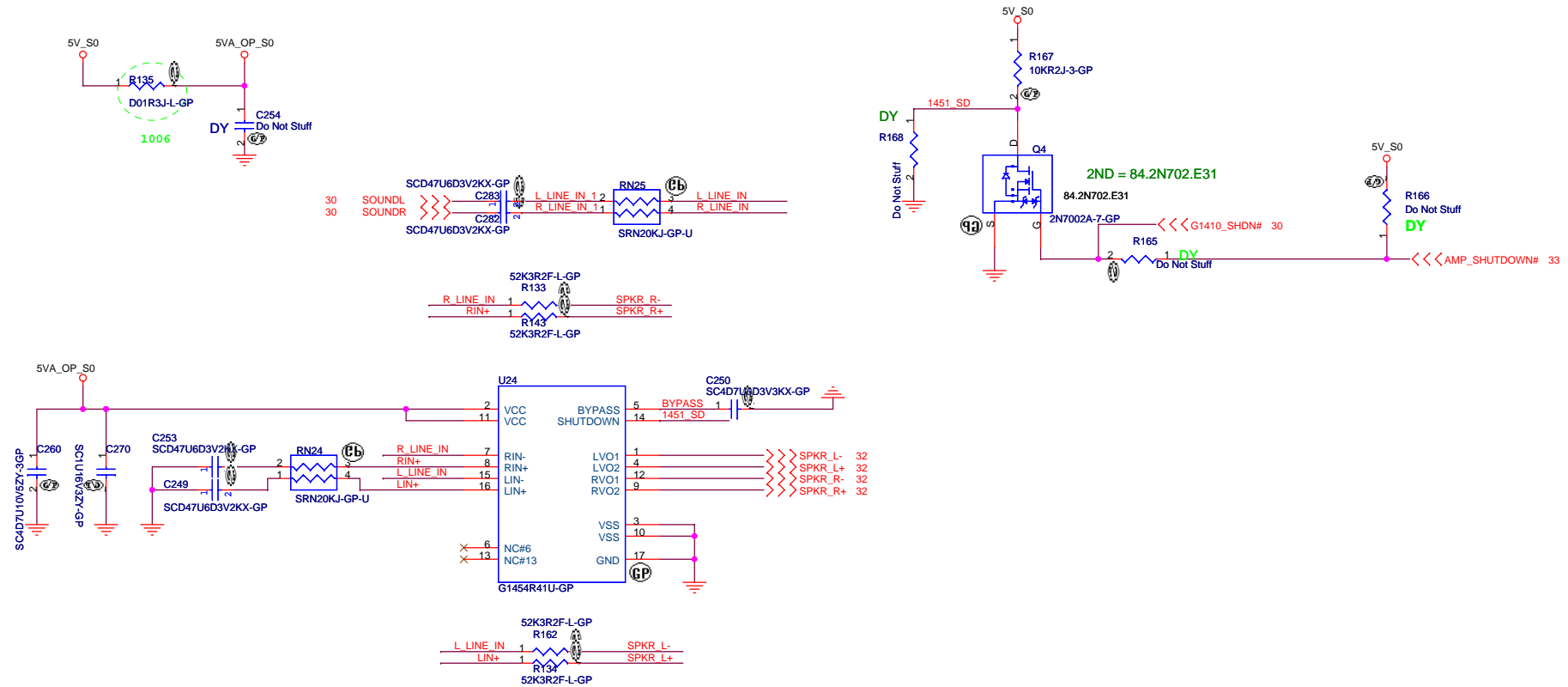
Title **Azalia codec ALC268**

Size A3	Document Number SM30	Rev SA
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Date: Saturday, October 18, 2008

Sheet 30 of 45

AUDIO OP AMPLIFIER

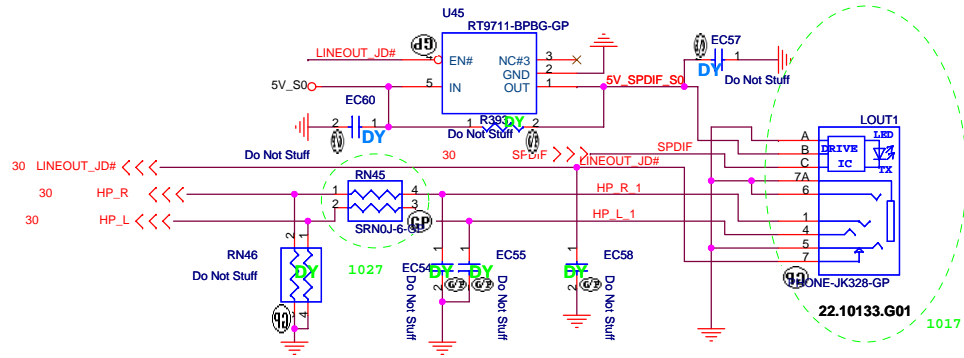


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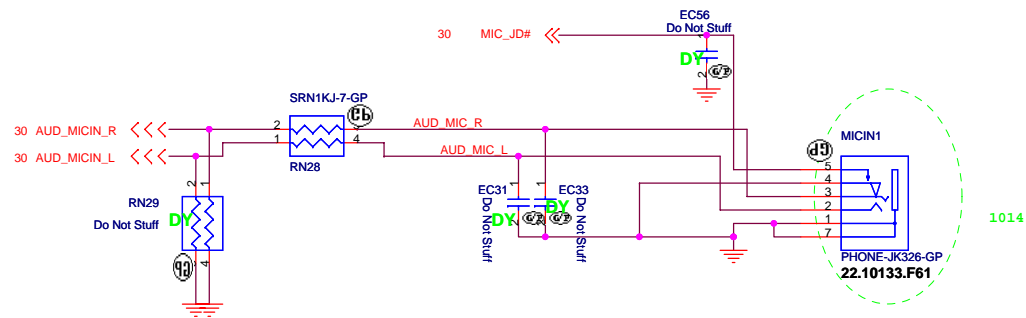
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		AUDIO AMP	
Size	Document Number	SM30	Rev SA
Date: Saturday, October 18, 2008		Sheet 31	of 45

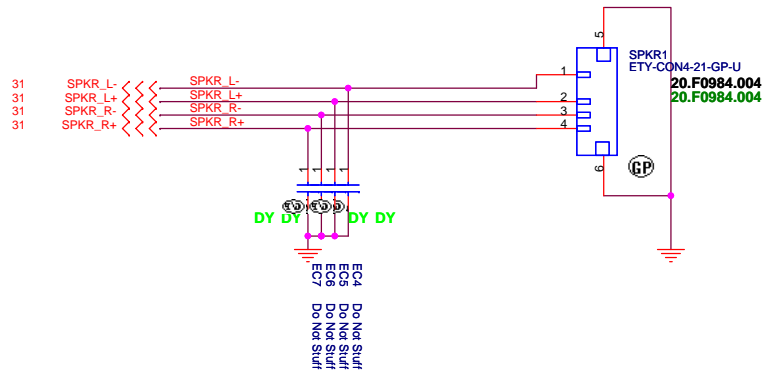
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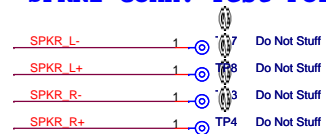
MIC IN



Internal Speaker



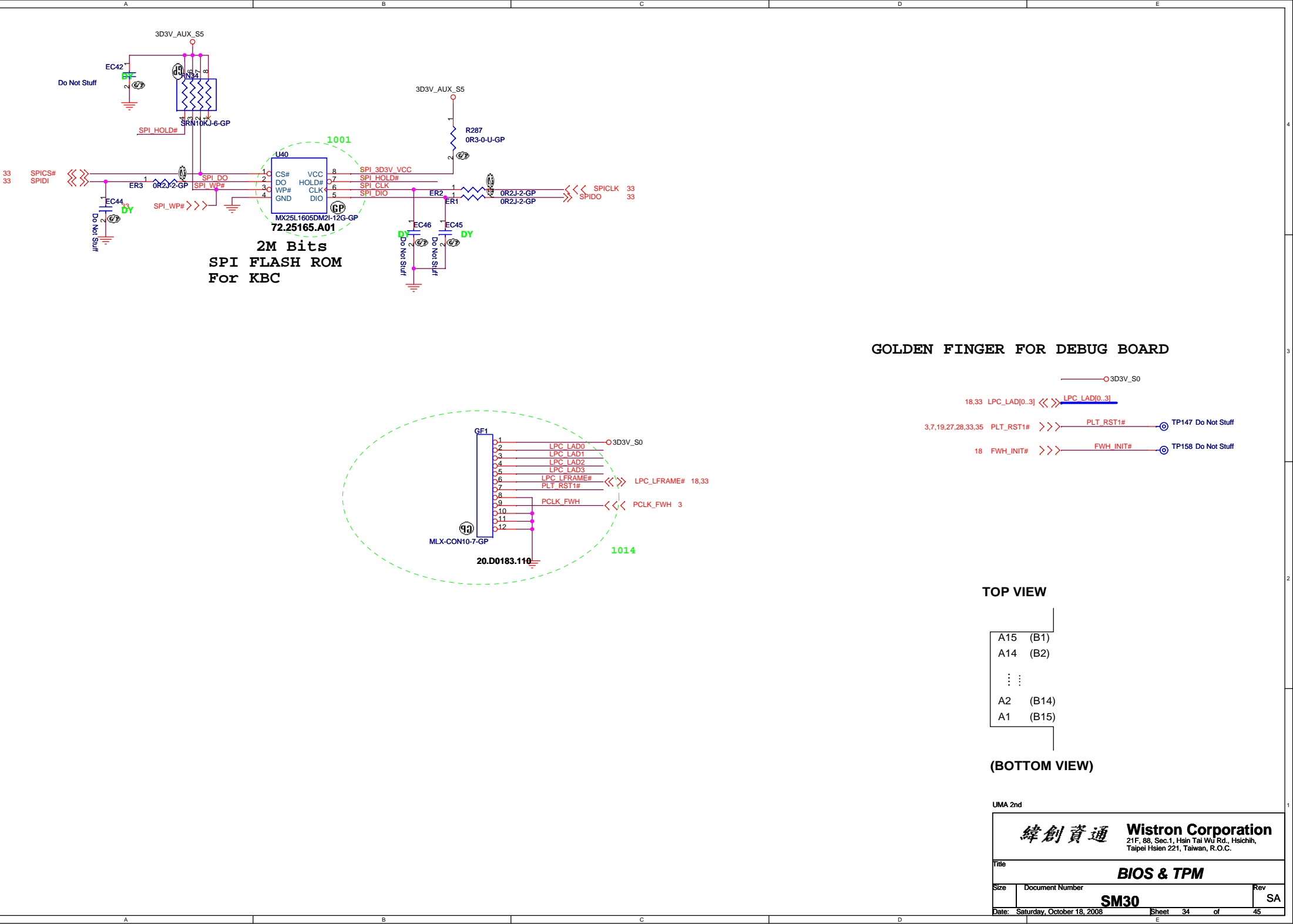
SPKR1 Conn. Test Point



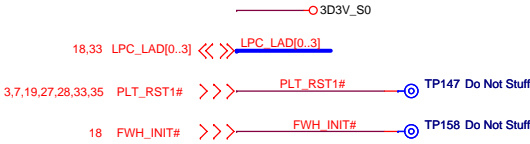
UMA 2nd

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

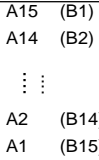
Title			
AUDIO JACK			
Size	Document Number	Rev	
	SM30	SA	
Date:	Monday, October 27, 2008	Sheet	32 of 45



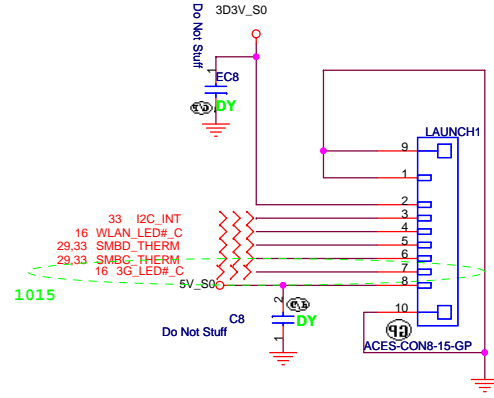
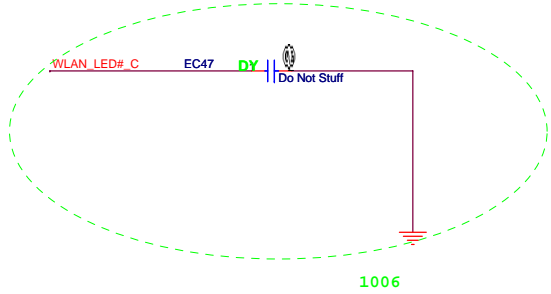
GOLDEN FINGER FOR DEBUG BOARD



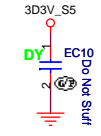
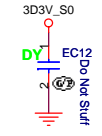
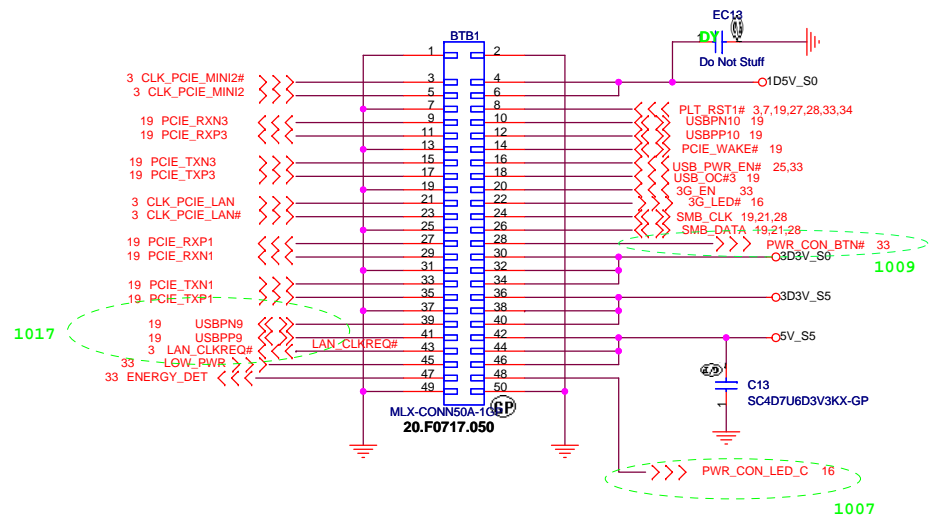
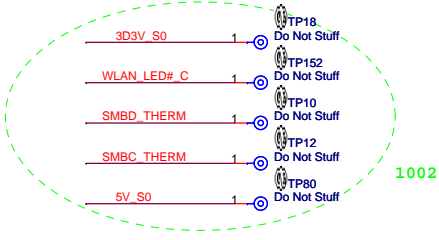
TOP VIEW



(BOTTOM VIEW)



LAUNCH Test Point



Aux Power

3D3V_AUX_S5

I min = 300 mA

U47

VIN VOUT

GND EN NC#4

RT9198-33PBR-GP

74.09198.G7F

2nd = 74.09198.G7F

3D3V_AUX_S5

3D3V_AUX_S5

3D3V_AUX_S5

3D3V_AUX_S5

3D3V_AUX_S5

3D3V_AUX_S5

3D3V_AUX_S5

3D3V_AUX_S5

3D3V_AUX_S5

3D3V_AUX_S5

3D3V_AUX_S5

3D3V_AUX_S5

3D3V_AUX_S5

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3D3V_AUX_S5

3D3V_AUX_S5

3D3V_AUX_S5

Run Power

2nd = 84.00610.D31

Q25 TP0610K-T1-GP

10KR2J-3-GP

10KR2J-3-GP

10KR2J-3-GP

10KR2J-3-GP

10KR2J-3-GP

10KR2J-3-GP

10KR2J-3-GP

10KR2J-3-GP

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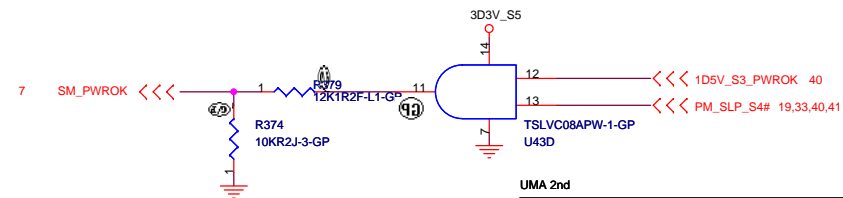
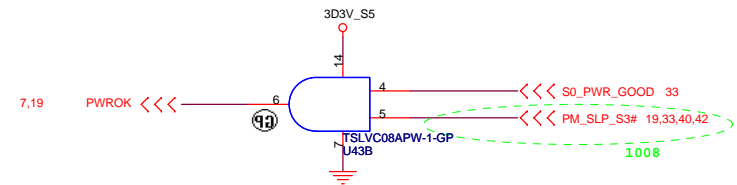
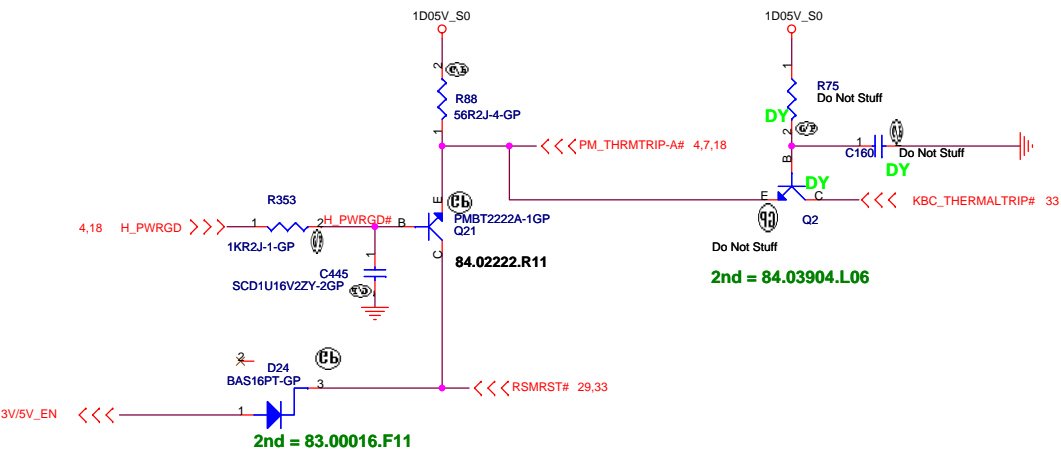
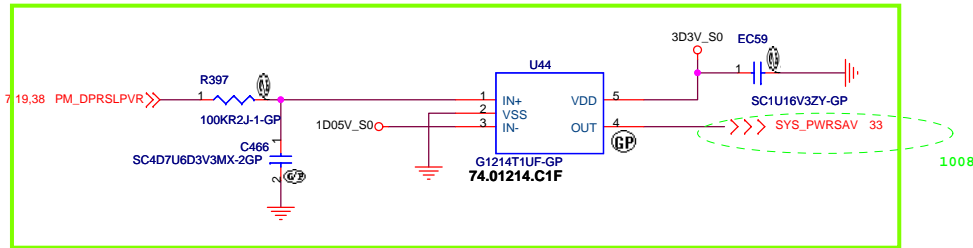
10KR2J-3-GP

10KR2J-3-GP

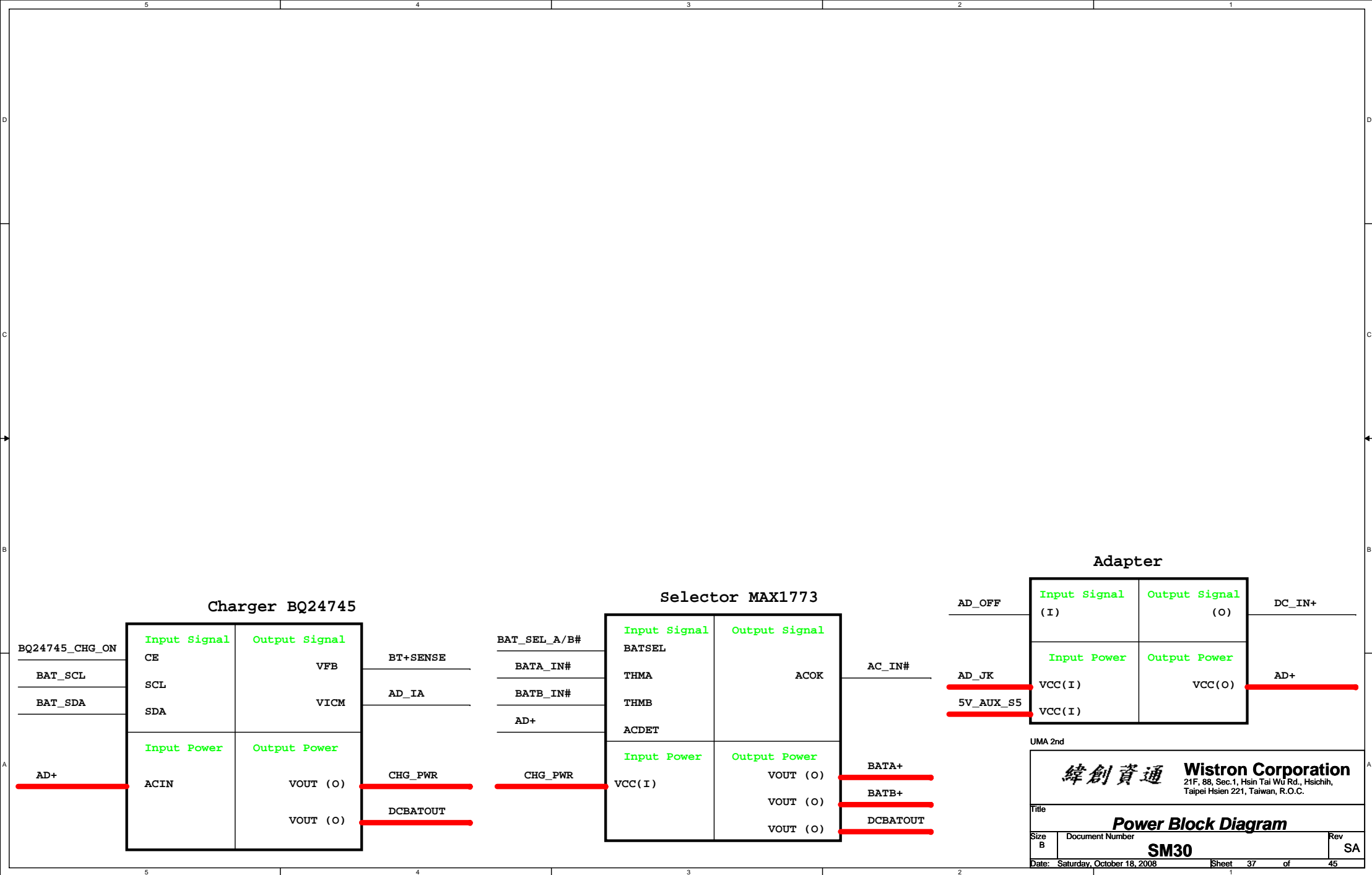
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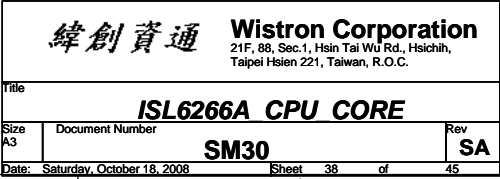
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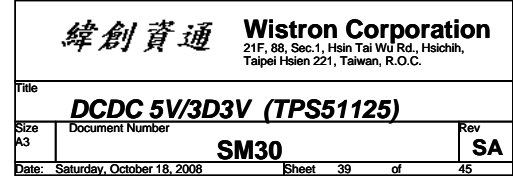
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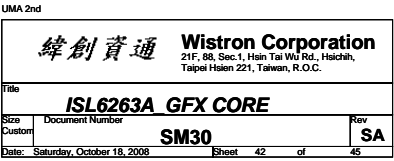


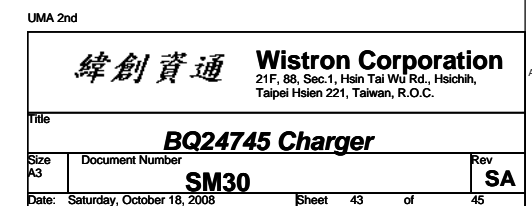
UMA 2nd

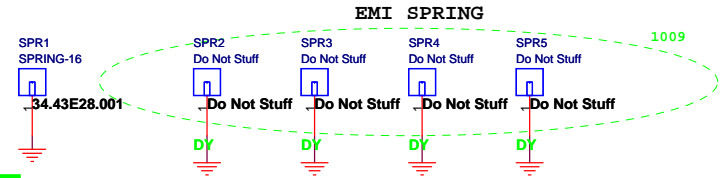
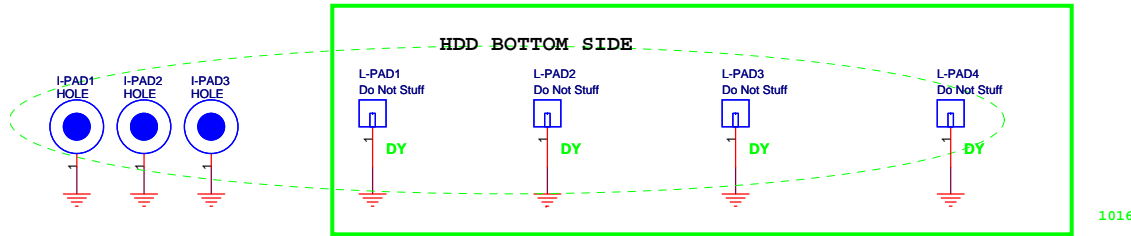
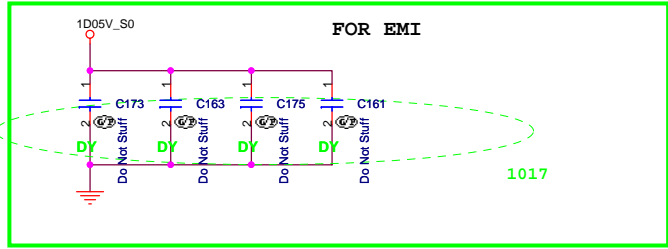












Stand off Location

